Radiant Technologies, Inc.
2835D Pan American Freeway NE
Albuquerque, NM 87107
Tel: 505-842-8007
Fax: 505-842-0366
e-mail: radiant@ferrodevices.com
www.ferrodevices.com

Application Note
Autonomous Memory
Rev A

Date: July 20, 2011

Author: Joe Evans

Introduction:
Radiant has developed a new circuit architecture that allows discrete ferroelectric capacitors to be used as electronic memories. The devices are known as autonomous memories because they do not require a microcontroller, a clock, or control lines to enable their read and write functions. The simplest electronic memory imaginable has the following functional diagram:

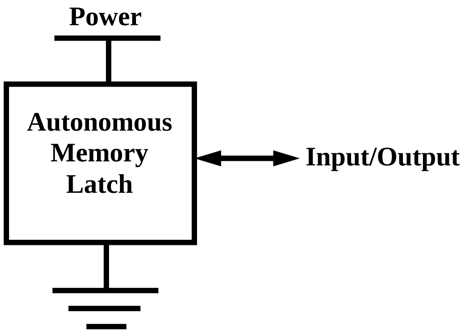


Figure 1: Function diagram of an autonomous memory

This memory operates with only two rules:

1) When power is applied to the circuit, the Output resumes the state it had before power was last removed.

2) The value of the Output may be changed by dragging it to the desired state *with or without* power.

In a perfect memory circuit, the Output could take on any state between Power and Ground, creating an analog latch. This document describes a more limited version of such a device where the Output is stable only at the values of Power and Ground, in other words an autonomous nonvolatile digital latch.

The purpose of this application note is to provide the circuit theory to allow an electrical engineer to design, build, and operate an autonomous memory. The memory circuit may be fabricated using any circuit technology including bipolar transistors, JFETs, MOSFETs, thin film transistors, relays, or exotic switches such as SCRs. The operation of the core non-latching autonomous memory will be introduced first followed by the addition of feedback paths to produce latching. The application note will close with recommended components and values to build simple latches using available discrete ferroelectric capacitors and a discussion of variations of the circuit to work in integrated circuits.

FeRAMs

A ferroelectric capacitor may be considered to be a charge generator with memory. A linear capacitor will always generate the same amount of charge for a given voltage application no matter its history. There is also a one-to-one correspondence between the voltage across the capacitor and the charge in a linear capacitor. At zero volts, there is zero charge. As a charge generator with memory, a ferroelectric capacitor stimulated by a fixed voltage will generate different amounts of charge depending on its history. It can also retain charge on its plates with zero volts measurable between the plates. In fact, the first thing most electrical engineers do when presented a polarized ferroelectric capacitor is to put a voltmeter across its plates! They then scratch their heads when it reads zero volts.

This memory property is utilized in a type of integrated memory circuit called an FeRAM. The acronym stands for **Fe**rroelectric **R**andom **A**ccess **M**emory. After 25 years of development, these IC memories are now sold by several companies including Ramtron, Fujitsu, Texas Instruments, and Matsushita. Other IC companies are considering entering this market but the cost of entry is quite high due to incompatibilities between the process steps required to form the ferroelectric materials on a silicon wafer and the standard process steps used to make integrated circuits on the same substrate. The companies mentioned above have solved this problem, leading to non-volatile IC memories that can be written or read in less 100 nanoseconds but retain for at least 10 years.

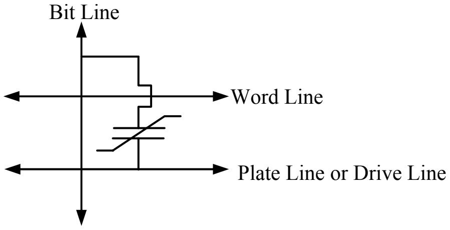


Figure 2: Simple FeRAM Memory Cell

Figure 2 above shows the circuit diagram for a single bit of memory in an FeRAM. This cell is passive and has no capability to operate itself. In a complete memory, thousands of these cells are arrayed horizontally along each Word Line and vertically along each Bit Line. The driver circuits and controls to read and write this passive cell are placed along the outside edge of the array of cells. There are many journal papers, textbooks, and magazine articles describing the intricacies of the operation of this FeRAM cell. In the simplest procedure, the direction of the ferroelectric capacitor can be written by

1) Turning on the MOSFET pass gate using the Word Line
2) Pulsing either a) Bit Line HIGH and Plate Line LOW or b) Bit Line LOW and Plate Line HIGH.
3) Turning off the Word Line

The state of the ferroelectric capacitor is cell is destructively read by

1) Turning on the MOSFET pass gate using the Word Line
2) Setting the Plate Line HIGH to force the ferroelectric capacitor to point towards the Bit Line. Either a large amount of charge or a small amount of charge will be deposited on the Bit Line depending on whether the ferroelectric capacitor switched or not. This wipes out the memory state of the ferroelectric capacitor.
3) Reading the amount of charge on the Bit Line by any of several methods.
4) Re-writing the original state of the ferroelectric capacitor.
5) Turning off the Word Line

This is a lot of activity to determine the state of one memory bit. To execute this activity requires a clock, a charge sensing circuit, and some sort of controller to coordinate the complex dance of the Bit Line, Word Line, and Plate Line. Despite their complexity, such control circuits can be efficiently implemented in integrated circuits *if* combined with large arrays of the memory cell in Figure 2. The typical Flash memory cell used in the ubiquitous Flash memory sticks has even more complexity since it requires high voltages to set the memory state and must generate these higher voltages on-chip.

For a ferroelectric capacitor to operate autonomously, it must eschew the complexity associated with the FeRAM. The circuit theory provided in the next section describes a method to accomplish this objective.

Autonomous Memory Operation

For a single ferroelectric capacitor to operate as a memory element in an autonomous memory circuit, it must

1) eliminate any control lines and clocks,
2) be associated with some sort of device to sense its state, and
3) have a method of changing its state.

Without externally clocked control lines, the only signal available to execute a read operation is the application of power to the circuit. There are a variety of simple electronic circuits that may change their state in response to the charge coming out of a ferroelectric capacitor. Specifically, any type of transistor can be combined with a ferroelectric capacitor to produce variable impedance. One such circuit using a bipolar NPN transistor as the detector and a resistor to translate the memory state is shown in Figure 3.

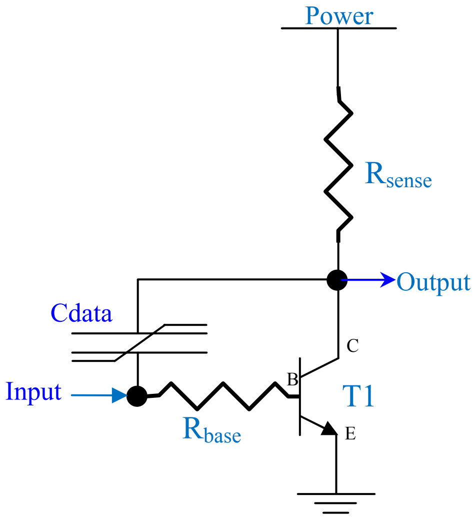


Figure 3: Destructively read autonomous memory circuit.

The description below ignores how the value of the ferroelectric capacitor was set before the read operation takes place. The read operation for the circuit in Figure 3 is 1) destructive, i.e. the data is destroyed by the read operation, and 2) not restorative. Starting when power is off, the ferroelectric capacitor C_{data} is either in the saturated UP or saturated DOWN state where UP points to Power through R_{sense}. When Power is applied, it charges C_{data} through R_{sense}, R_{base}, and the PN diode of T1 as shown in Figure 4. Eventually, C_{data} will reach the saturated UP state.

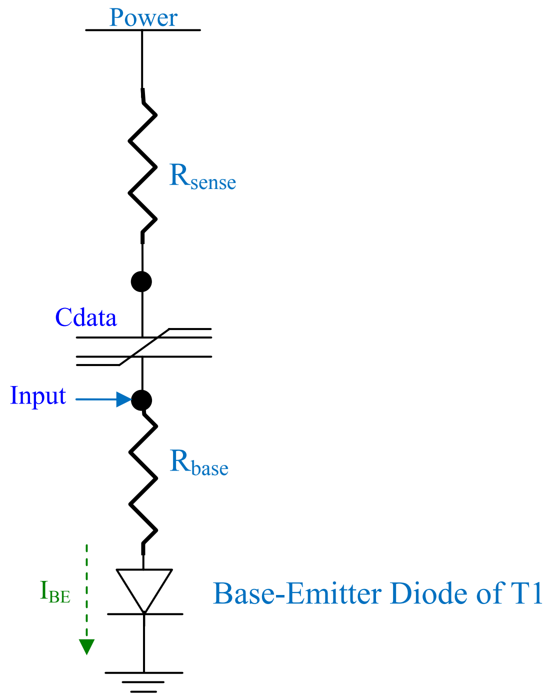


Figure 4: Equivalent circuit for charging the ferroelectric capacitor UP.

The current arising from the ferroelectric capacitor passes through the base-emitter diode of T1, forcing a larger current through the collector-emitter circuit of T1 by the factor of

$$I_{CE} = \beta \text{ x } I_{BE} = \beta \text{ x } I_{FE} \qquad \text{Eq(1)}$$

See the figure below.

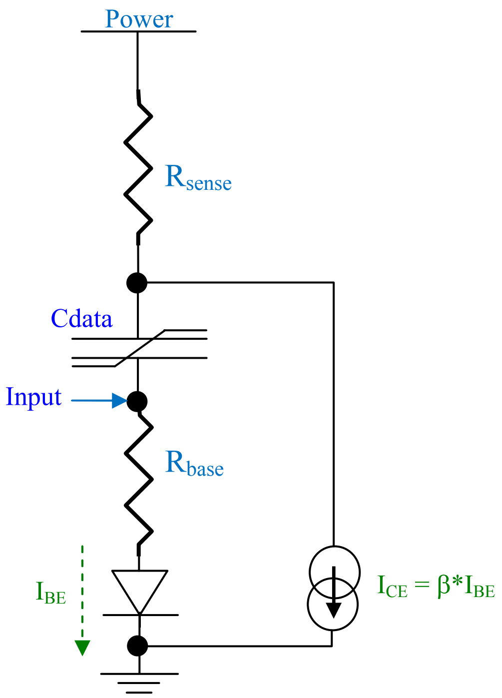


Figure 5: Equivalent circuit for current flow through the circuit.

Therefore, the current through R_{sense} in Figure 4 above becomes

$$I_{sense} = I_{FE} + \beta \text{ x } I_{FE} \qquad \text{Eq(2)}$$

$$I_{sense} = I_{FE}(1 + \beta) \qquad \text{Eq(3)}$$

The current through R_{sense}, on the other hand, determines the voltage drop across R_{sense} and thus the voltage across the ferroelectric capacitor.

$$V_{FE}(t) = V_{Power} - V_{sense} - I_{FE}\, R_{base} - V_{th(PN)} \qquad \text{Eq(4)}$$

$$V_{FE}(t) = V_{Power} - V_{sense} - I_{FE}\, R_{base} - 0.7V \qquad \text{Eq(5)}$$

For simplicity, assume that the power ramps from zero to its maximum value at a constant rate. Equation 5 may then be rewritten to Equation 6.

$$V_{FE}(t) = \frac{dV_{Power}}{dt} * t - (1 + \beta)\, I_{FE}\, R_{sense} - I_{FE}\, R_{base} - 0.7V$$

$$V_{FE}(t) = \frac{dV_{Power}}{dt} * t - I_{FE}\,[\,(1+\beta)\,R_{sense} + R_{base}\,] - 0.7V \qquad Eq(6)$$

The output of the circuit in Figure 3 is the power voltage minus the voltage drop across the sense resistor.

$$V_{Output} = \frac{dV_{Power}}{dt} \bullet t - (1+\beta) I_{FE}\, R_{sense} \qquad Eq(7)$$

Equation 7 is the key to understanding the autonomous circuit in Figure 3. The current generated by the ferroelectric capacitor, I_{FE}, depends upon the value of V_{Output} as well as *the remanent polarization state of the ferroelectric capacitor*. A measure of the charge generated by a ferroelectric capacitor as a function of voltage illustrates the point. Figure 6 shows the hysteresis loop for a Radiant Technologies, Inc. Type AB capacitor consisting of Lead Zirconate Titanate between top and bottom planar platinum electrodes. The WHITE designation indicates the planar area of the capacitor, in this case 10,000 square microns.

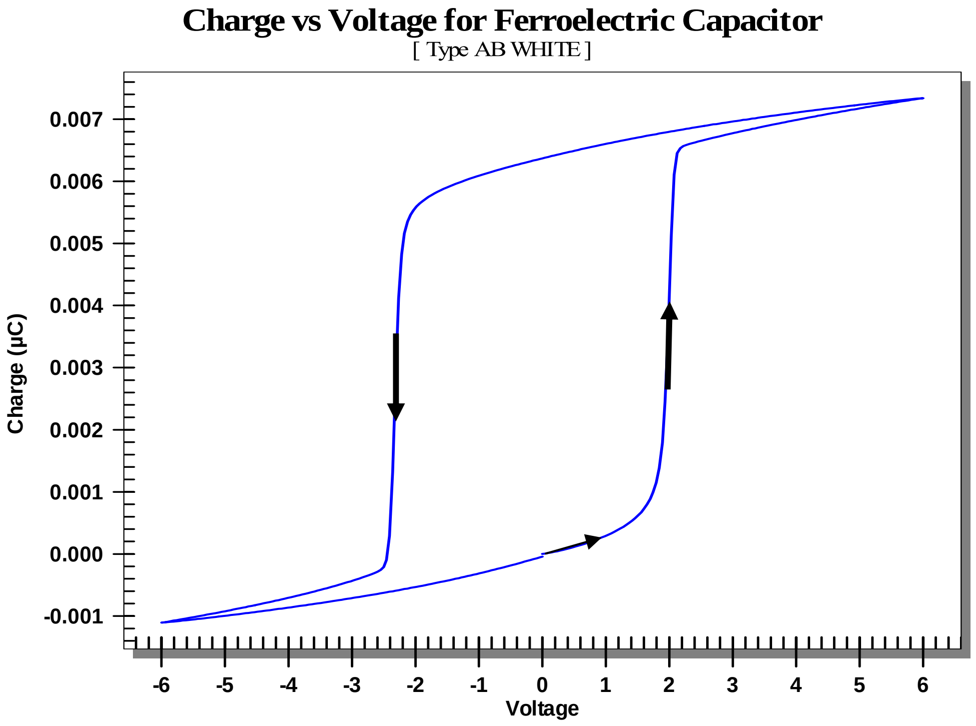


Figure 6: Polarization vs voltage loop for a ferroelectric capacitor.

The horizontal axis of the plot is the voltage applied across the capacitor. The vertical axis is the sum of all charge that has come out of or gone into the capacitor at each voltage on the X-axis since the beginning of the test. The vertical axis is labeled in microcoulombs which is 1×10^{-6} coulombs. Remember that 1 microcoulomb is generated by 1 volt across a 1 microfarad capacitor. What is the capacitance of the ferroelectric device in Figure 6? The mathematical derivative of the data in Figure 6, shown in Figure 7, yields the instantaneous capacitance of the device at each voltage.

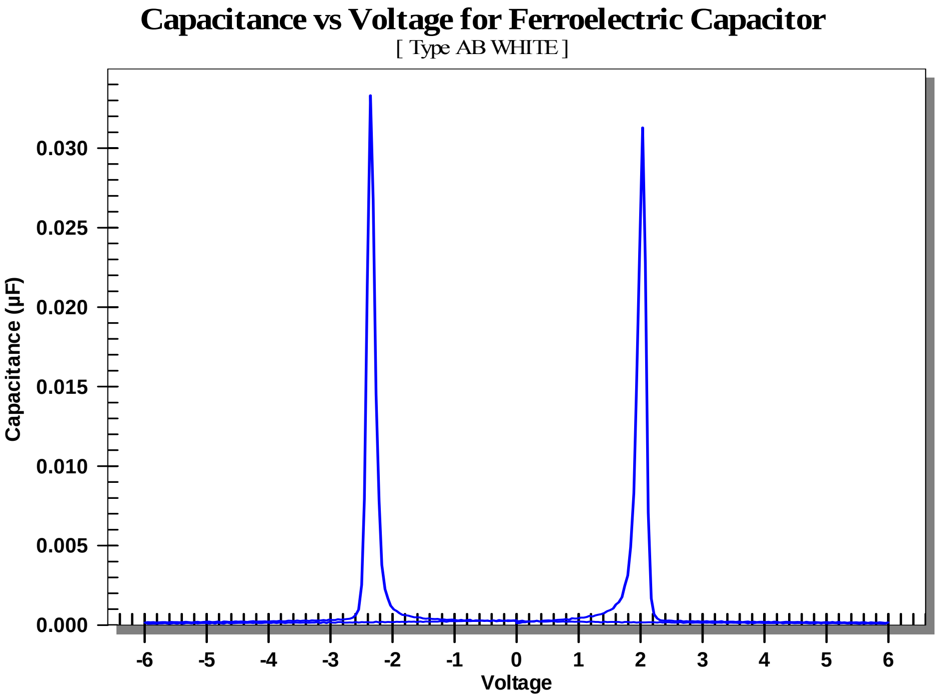


Figure 7: Instantaneous capacitance vs voltage for the ferroelectric capacitor in Figure 6.

The capacitance on the plot in Figure 7 is in units of microfarads. It peaks at 33.3nF during the switch. If the capacitor does not switch, the "humps" in the derivative will not occur, leaving a small capacitance in its place. The non-switching capacitance of the device is magnified in Figure 7a and is approximately 0.25nF, more than a 100 times difference!

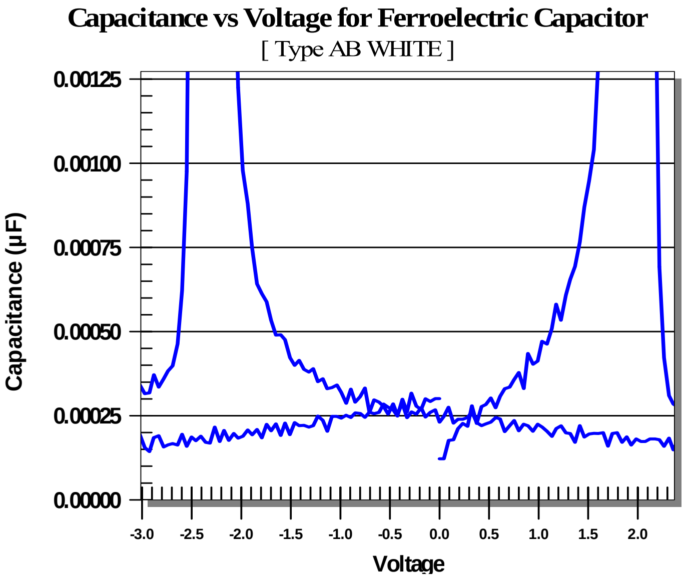


Figure 7a: Non-switching capacitance for the device in Figure 5.

A simple way to model the ferroelectric capacitor in Figures 7 and 7a is with two linear capacitors, one much larger than the other. The smaller capacitor is the *non-switching* capacitor while the larger capacitor is the *switching* capacitor. Always maintaining the capacitor fully UP or fully DOWN during retention results in two possible capacitance vs volts profiles when a positive voltage is applied to the power terminal of the memory circuit in Figure 3:

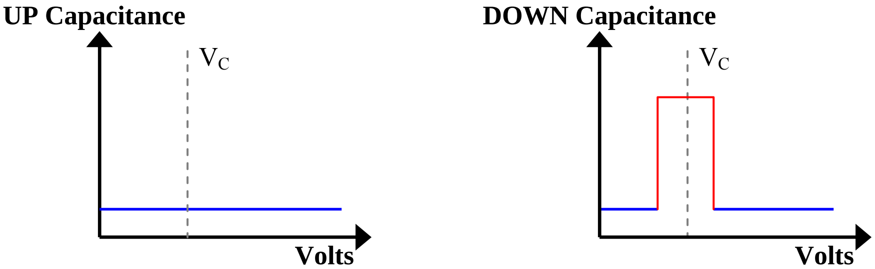


Figure 8: Simple Capacitance vs Voltage model for ferroelectric capacitor.

What would be the behavior of the circuit in Figure 5 given the two linear capacitances the ferroelectric capacitor will generate from the DOWN state when power is applied to the circuit? If the complex current from the ferroelectric capacitor in Equation 7 is replaced with the simple current equation of a linear capacitor and we assume that β >> 1, Equation 7 reduces to the following:

$$V_{Output} == \frac{dV_{Power}}{dt} \bullet t - \beta R_{sense} I_{linear\ cap}$$

$$V_{Output} == \frac{dV_{Power}}{dt} \bullet t - \beta R_{sense} C_{data} \frac{dV_{Output}}{dt} \qquad \text{Eq(8)}$$

Equation 8 can be used to approximate the behavior of the circuit in Figure 3. The coefficient value [$\beta R_{sense} C_{data}$] controls this circuit. It consists of the β of the transistor times the RC time constant of R_{sense} and C_{data} in Figure 5. It has units of time and can be viewed as the amplified time constant of R_{sense} and C_{data}. Because the output voltage in Equation 8 *depends upon its own rise time*, this equation can have complex behavior. It is easiest to analyze at two extremes. If βRC is much slower than the ramp rate of the power voltage, i.e. the rise time of the capacitor is much slower than the rise time of the power, the output node will fall further and further behind the power voltage as the power voltage rises. This will lead to a slow exponential rise of the output voltage. On the other hand, if βRC is faster than the ramp rate of the power voltage, i.e. the rise time of the voltage across C_{data} given the value of βR_{sense} is faster than the rise time of power, βRC can be treated as a small constant. In that case, taking the derivative of Equation 8 yields the following relationship between the ramp rate of power and the ramp rate of the output voltage.

$$\frac{dV_{Output}}{dt} = \frac{dV_{Power}}{dt} \qquad \text{Eq(9)}$$

The ramp rate of the output will be the same as the ramp rate of the power. Substituting Equation 9 back into Equation 8 yields the behavior we are looking for:

$$V_{Output} = \frac{dV_{Power}}{dt} \bullet t - \beta R_{sense} C_{data} \left(\frac{dV_{Power}}{dt}\right)$$

$$V_{Output} = \frac{dV_{Power}}{dt} \bullet [t - \beta R_{sense} C_{data}] \qquad \text{Eq(10)}$$

V_{Output} will follow the power with a constant gap set by $\beta R_{sense} C_{data}$. Finally, we can calculate the voltage drop across R_{sense}.

$$V_{sense} = V_{Power} - V_{Output} = \frac{dV_{Power}}{dt} \bullet t - \left[\frac{dV_{Power}}{dt} \bullet t - \beta R_{sense} C_{data} \left(\frac{dV_{Power}}{dt}\right) \right]$$

$$V_{sense} = \beta R_{sense} C_{data} \left(\frac{dV_{Power}}{dt}\right) \qquad \text{Eq(11)}$$

Equation 11 is easy to interpret. The value of V_{sense}, the voltage across R_{sense}, will be set by the value of C_{data} in the equation. If C_{data} has the non-switching value, V_{Output} will follow V_{Power} at a small voltage difference below V_{Power}. If the ferroelectric capacitor begins in the DOWN position, it will initially have the value of the non-switching capacitor but will change to the higher switching capacitance when the voltage across the ferroelectric capacitor approaches its coercive voltage as modeled in Figure 8. The value of βRC will be much larger while remanent polarization is switching, causing the difference between the power and the output voltage to be much higher. After all of the remanent charge has been switched, the capacitor will return to its original low capacitance value, reducing the difference between the output voltage and power. Figure 8a gives a visual picture of Eq(11) in action for the two states. The **Green** trace in Figure 8a is the DOWN capacitance model of Figure 8 above. The BLUE trace is the output voltage during power-up if C_{data} begins in the UP state. The RED trace indicates what the Output will do if C_{data} begins in the DOWN state.

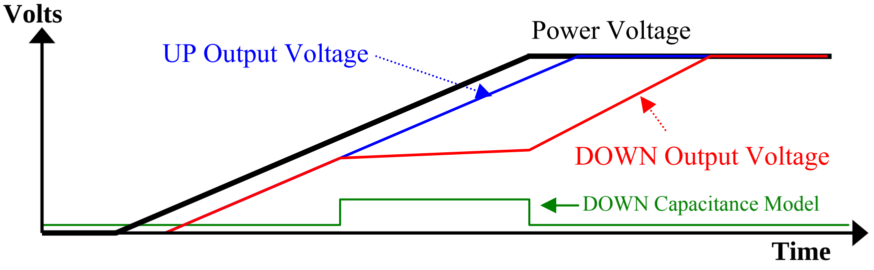


Figure 8a: Output voltage in time domain for both initial states.

Actual measurements of V_{Output} vs time for the circuit in Figure 3 are shown in Figure 9 and Figure 10 below. The measurements were made using a Radiant Precision Premier II ferroelectric tester to apply the power voltage (middle trace), to collect the charge through the transistor (top trace), and to measure the output voltage (bottom trace). Figure 9 shows the output voltage for the circuit when the ferroelectric capacitor starts UP before power is applied. Figure 10 shows what happens when the ferroelectric capacitor starts DOWN.

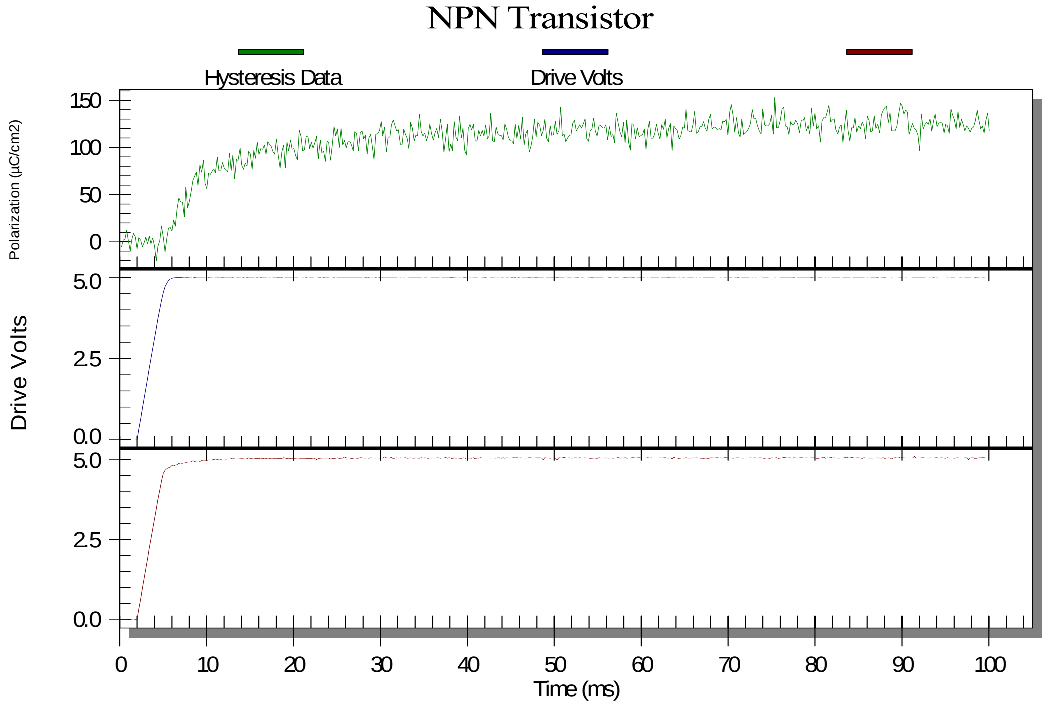


Figure 9: V_{Output} (bottom trace) when the ferroelectric capacitor starts UP

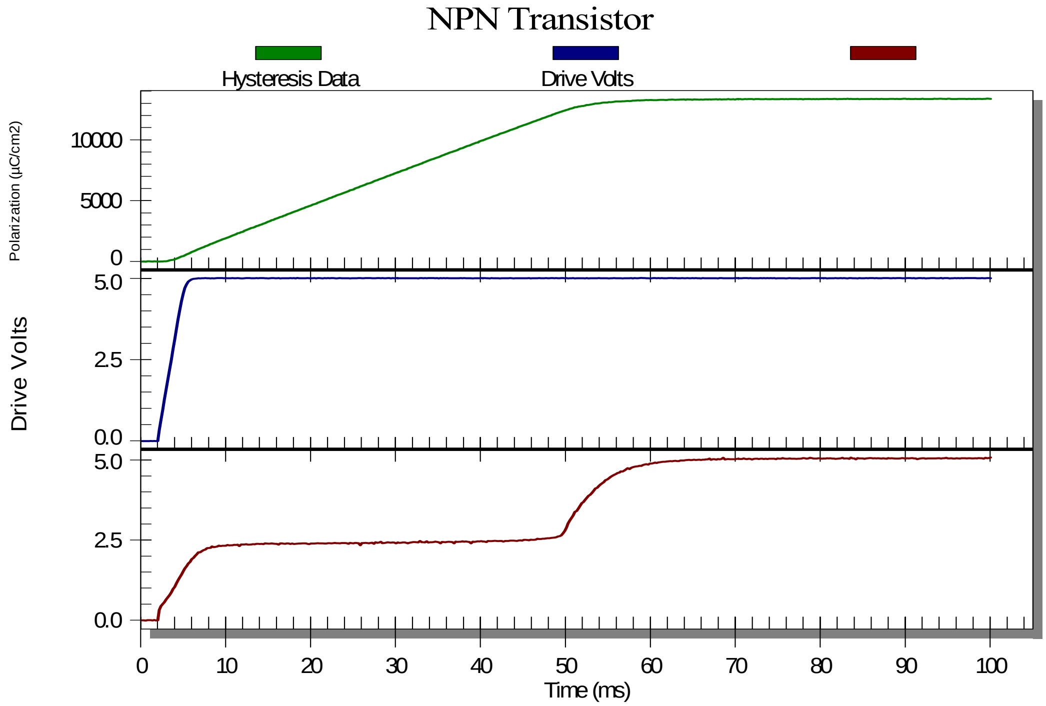


Figure 10: V_{Output} (bottom trace) when the ferroelectric capacitor starts DOWN

The capacitor in Figure 6 was used to operate the circuit measured in Figures 9 and 10. The difference between the switching and non-switching capacitance for this ferroelectric capacitor *almost turns the transistor off when switching starts.* However, it cannot turn the transistor totally off or no current will flow through the base-emitter circuit of the transistor. In reality, the feedback of the ferroelectric capacitor current and the transistor conduction current forces the output voltage to rise just fast enough to maintain a constant charge coming out of the ferroelectric capacitor until all of the switching charge is gone. Once the capacitor is totally switched, it reverts back in value to the non-switching capacitance and quickly catches up with the power voltage. The result is a "shelf" in the output voltage in Figure 10 that does not occur in Figure 9.

> N OTE: it is possible to envision a circuit where the transistor gain is so high the output voltage *oscillates* as the ferroelectric capacitor switches.

The charge that passes through transistor T1 in the top trace of Figure 10 has a constant slope to it, meaning that the negative feedback circuit formed between the voltage across the transistor collector-to-emitter path and the ferroelectric switching current flowing into the transistor base-to-emitter path forces *constant current* switching of the ferroelectric capacitor.

A very important feature of the plots in Figures 9 and 10 is that no matter what state the capacitor was in before power was applied to the circuit, the ferroelectric capacitor is *always in the UP state after power up.*

Writing the State:

The circuit in Figure 3 is put into the UP state by completing a read operation. To put the circuit in the DOWN state, take the Input node to the power voltage. The voltage on that node will force current through the base of the transistor, turning it on. With the transistor on, the ferroelectric capacitor can switch to the DOWN state with its switching current flowing to ground through the transistor. It is important to note that V_{Power} at the top of R_{sense} is not involved in writing the DOWN state into the ferroelectric capacitor and can be at ground potential or disconnected during the DOWN write operation.

Creating a Latch:

Now that the operation of the circuit in Figure 3 is understood, that circuit can be converted to a latch by adding a feedback circuit. The previous section demonstrated that if the capacitor was DOWN prior to power up, the shelf voltage occurs but if the capacitor was UP prior to power up the shelf voltage does not. The feedback circuit added to the circuit in Figure 3 should latch the DOWN state if the shelf voltage occurs but let the circuit stabilize UP if the shelf voltage does not occur. The feedback circuit must serve the second purpose of re-writing the DOWN state back into the ferroelectric capacitor.

The feedback circuit must compare the output voltage to some sort of reference to decide whether to latch the circuit DOWN. The circuit is latched DOWN by permanently turning on Transistor T1 in Figure 3. If T1 is left off, the output voltage will rise until it is stable in the UP state. The feedback circuit must compare the output voltage to some sort of reference to decide whether to latch the circuit DOWN. The voltage drop across R_{sense} can be used as the voltage reference for latching. By adjusting R_{sense} relative to the value of C_{data} in Figure 3, the rise time of the UP state in Figure 8a can be forced to generate only a small voltage across R_{sense} during the rise while the DOWN state would generate a much larger voltage across R_{sense}. Figure 8a then becomes Figure 11 where the output voltage for the UP state practically equals the power voltage but the output voltage for the DOWN state significantly deviates from the power voltage during power up.

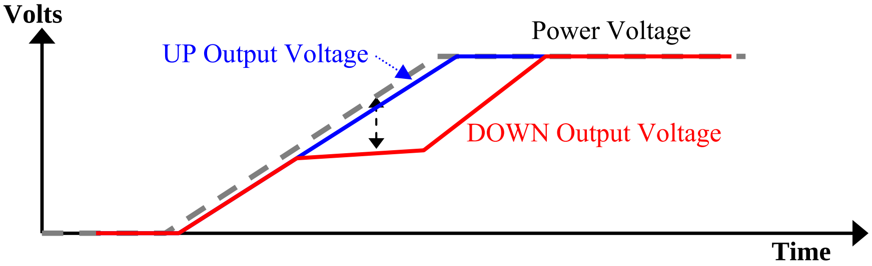


Figure 11: Output voltage with fast rise time.

Figure 11 shows that if the ferroelectric capacitor is in the DOWN state before power is applied, a significant difference will develop between the power voltage and the output voltage as the power voltage rises. The feedback circuit should detect this difference when it occurs and turn on T1 to force the output voltage back to ground as in Figure 12.

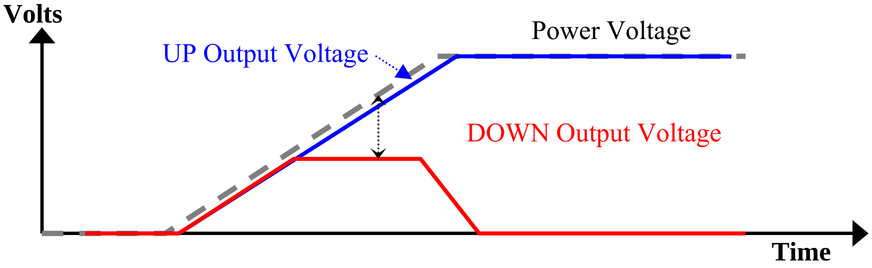


Figure 12: Output voltage latches to ground if the shelf voltage occurs.

One such feedback circuit uses the threshold voltage of another transistor T2 to control the base of the first transistor T1.

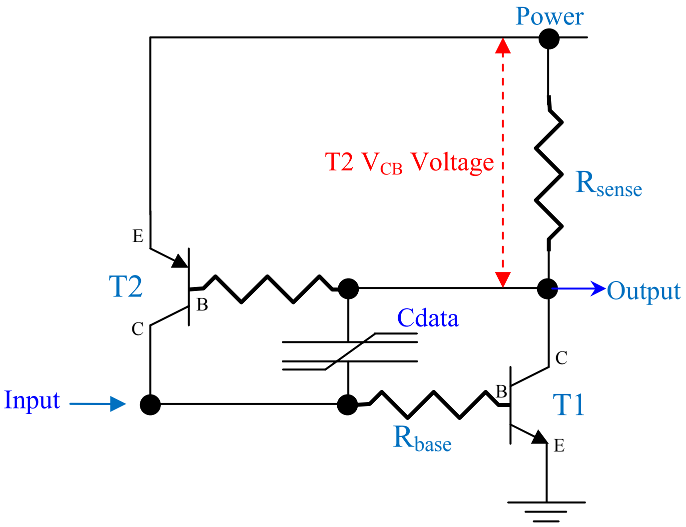


Figure 13: Adding a feedback transistor to the memory bit to form a latch.

T2 is a PNP bipolar transistor, the opposite type of transistor as T1. It remains off unless the voltage across R_{sense} exceeds the V_{BE} threshold of the base-to-emitter diode, approximately 0.7V in the direction from the emitter to the base. Figure 12 shows the two possible paths for the output voltage. With the value of R_{sense} selected correctly versus the rise time of power and the size of C_{data}, the UP state will not generate enough voltage across R_{sense} to turn on T2. T2 remains off as the output voltage rises to eventually match the power voltage. With T2 off, T1 also remains off and a stable condition is maintained as long as power is supplied. If the latch starts in the DOWN state, the output voltage will begin to lag further behind the power voltage when C_{data} begins to switch. When the differential across R_{sense} exceeds 0.7V, T2 will turn on, forcing T1 on as well. The conduction of T1 will force the output voltage low, latching T2 and T1 into the conductive state. This condition is also stable as long as power remains supplied to the latch.

Three interrelated factors control the operation of the circuit in Figure 13:

1) The time constant of R_{sense} and C_{data}
2) The rise time of the $V_{Power.}$
3) The absolute values of R_{sense} and C_{data} selected so
    a. Non-switching ferroelectric current generates much less than 0.7V across R_{sense}.
    b. Switching ferroelectric current will generate more than 0.7V across R_{sense}.

The circuit in Figure 13 *re-writes the original state back into* C_{data}*!* If C_{data} is programmed UP before power is supplied, once the circuit settles on the output voltage will equal the power voltage, reinforcing the UP state in C_{data}. The DOWN state is different. With both T2 and T1 on, C_{data} will be forced back into the DOWN state. T2 will pull its DOWN terminal to the power voltage, while T1 will pull its UP terminal to ground! Trace the direction of the voltage through C_{data} for both the latched UP and latched DOWN states to visualize the direction of the re-write by the circuit.

In summary, the latch circuit in Figure 12 will read the value of C_{data} and set the Output to a value to match the state stored in C_{data}. The circuit will, at the same time, restore C_{data} to the original value it had before power was applied. The circuit executes the read operation on power-up of the function block in Figure 1.

Writing a New State:
A new state may be written to C_{data} *with power on or off*. With power applied, either the input or the output denoted in Figure 13 may be dragged to the opposite state by an external circuit or switch to change the status of T2 and T1 and effectively latch the circuit into the opposite direction. As noted above, the new latch condition will be automatically written into C_{data} by the circuit and recalled on the next power-up cycle. Note that the Output and the Input have opposite states to each other.

The power consumption required to pull the Input down while T2 is on or pull the Output up when T1 is on would be quite high. Small resistances may be placed strategically to reduce the power required to change the latch state. In Figure 14, R_{in} has been added to the input to provide a moderate input resistance for an input of either direction independent of the state of T2. A similar resistor could be placed between T1 and V_{Output} but a better method would be to set the value R_{base} to limit the drive capability of T1 to less than that of the external circuit that attempts to move the output node to the desired state. Note that the value of R_{in} in this location must be balanced against the value of R_{sense} to ensure that the latch still properly reads C_{data} on power up. A third method would be to attach the input control line to the base circuit of T2 to accomplish low power write operations.

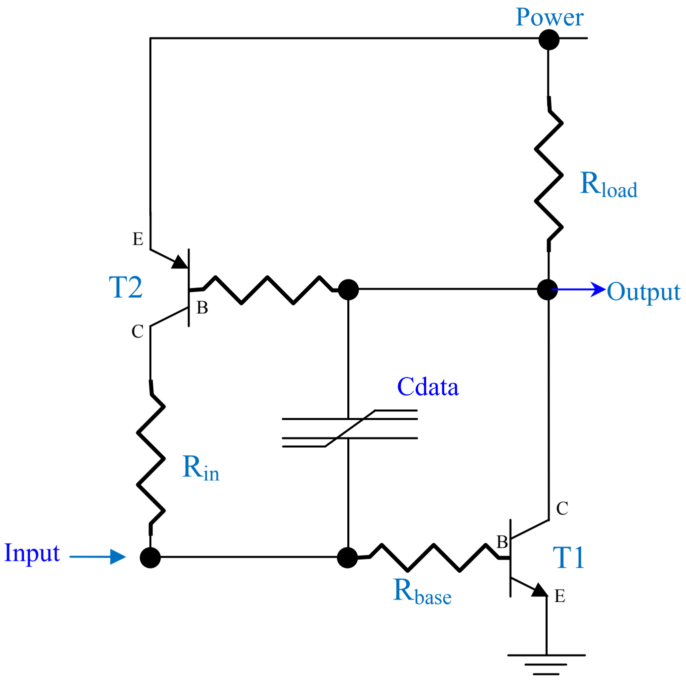


Figure 14: R_{in} limits the power required to change the state of the latch with power applied.

In Figure 14, if T1 is off, the Output will be high and C_{data} will be UP. Pulling Input to Power will turn on T1 which in turn will turn on T2, force Output low, and re-write C_{data} to the DOWN state. From the DOWN state, Input may be pulled to ground to force T1 off which will turn off T2, allow Output to rise to the Power level, and re-write C_{data} to the UP state.

A very important aspect of the input is that when not intended to be used, the Input signal *must be high impedance* so as not to affect the state of the latch. Therefore, two input controls are needed to control the autonomous latch: the IN data and a switch to connect the IN data to the latch. Or, two separate 2-state inputs may be brought in where the two states are ACTIVE and HI-Z: one state is LO/HiZ while the other is HI/HiZ.

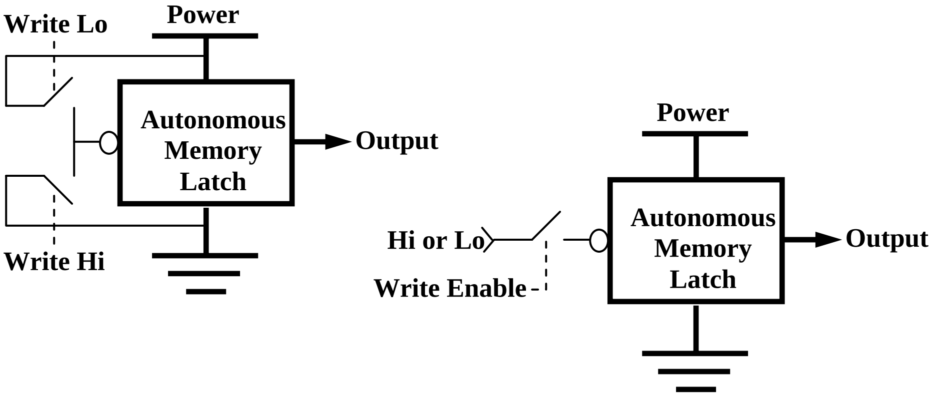


Figure 15: High impedance inputs.

No-Power Writes

An interesting property of the circuit in Figure 13 is that *it may be written with the power off!* Thus, the ferroelectric capacitor could be used to detect a change in state for an external object *while power to the circuit is off.* The state of the ferroelectric capacitor will then be latched by the circuit on the next power cycle. With the Power line connected to ground or floating electrically, a voltage on the Input will force the DOWN terminal of C_{data} high while also turning on T1 to pull the UP terminal of C_{data} low. This writes a DOWN state in the capacitor. By the same token, a voltage applied to the Output node will pull the UP terminal of C_{data} high. The DOWN terminal of C_{data} will be connected to ground through the base circuit of T1. The external object executing the power-off write must be able to generate enough voltage *as well as* enough charge to switch C_{data} .

This unique property leads to the interesting application where no power is applied to the circuit during sensing. C_{data} should already be preset UP. A sensor attached the Input is designed to apply sufficient power to the Input node to switch C_{data} DOWN should an event occurs that the sensor monitors. A microcontroller, or RFID transmitter, could then power up the latch at a later time and read Output to determine if the event occurred during the sleep period. For instance, ZIGBEE transceivers are designed to talk to each other via radio frequency to form mesh networks that pass information to/from a central controller at a distance. To save power, ZIGBEE nodes spend most of their time in the sleep mode. Internal timers wake up the transceiver on a schedule set by the remote controller to make measurements and pass those measurements to the remote controller. The autonomous memory latch can detect the occurrence of events *while the ZIGBEE transceiver sleeps* and then report the occurrence of the event to the node when it awakens.

Bipolar vs Other Technologies

The autonomous non-volatile latch circuit described above can be fabricated using any electronic technology both discrete and integrated. The advantage of this circuit is that *it does not require a supervisory microprocessor to read, write, or change state*, eliminating the necessity of a regulated power supply, software development, clock generation, etc., that would run up the cost of a single bit of traditional memory. Bipolar transistors were used in the sample circuits of this application note because they are available, easy to work with, and do not suffer from static discharge during handling. The non-volatile latch functionality can be achieved with a variety of other technology types including MOSFET, JFET, and even thin film transistors (TFTs) having ferroelectric gate oxides!

The resistance of R_{sense} may also be accomplished with some type of transistor. The variable impedance of the transistor can be set so that it has the value of R_{sense} to make the read operation successful but then change to higher or lower values when the circuit is stable to optimize output impedance while significantly reducing static power consumption. A classic example would be to replace R_{sense} with a resistor/JFET combination as shown in Figure 15. An n-channel JFET normally has low resistance when its gate voltage equals its source and drain voltages, i.e. when the circuit is off. The transistor turns off if the gate voltage becomes negative relative to the source and drain. In the non-volatile latch of Figure 15, the JFET gate is connected to the output voltage and automatically adjusts its conduction based on the state of C_{data}. The resistor between the Output and the JFET ensures that the gate goes negative relative to the transistor source and drain should the Output latch low, turning off the transistor and preventing significant current flow in the circuit from power to ground through T1. Should Output latch high, the JFET will be conductive, creating a low impedance output for the high state. Since this is a discrete circuit, we have the freedom to mix and match technologies as in Figure 16.

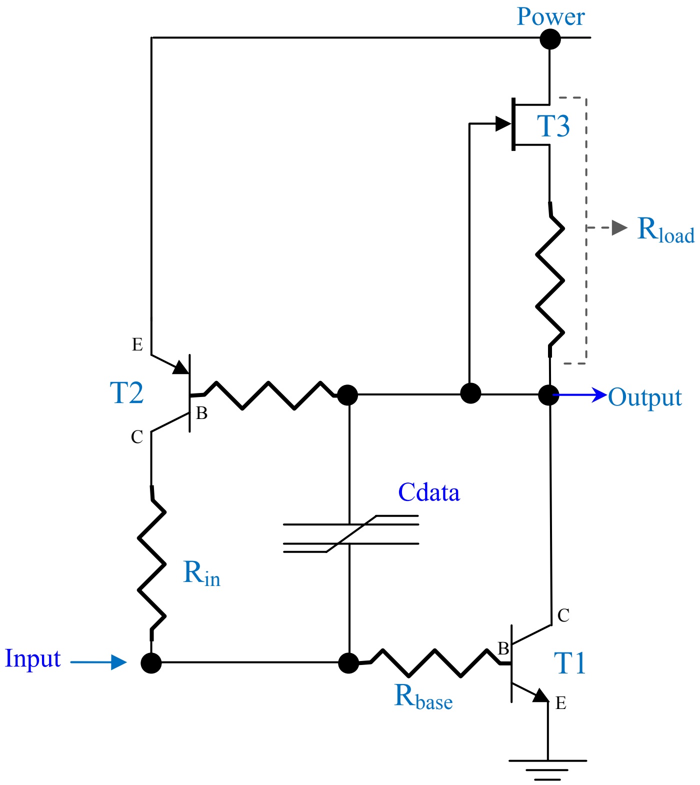


Figure 16: NV latch with variable R_{Load}.

Charge-based Read Circuit

The bipolar circuits in Figures 13 and 16 depend upon the current flow from the ferroelectric *through the base circuit* of the bipolar transistor T1 to modulate the state of the latch during power-up. A charge-based method may be employed instead. The charge-based method will function with a bipolar transistor in the T1 position but is absolutely necessary when using a FET in the T1 position since current will not flow into the gate and the ferroelectric capacitor requires a current path to ground.

For those familiar with ferroelectric measurements, a Sawyer-Tower circuit is constructed around the base or gate circuit of T1. For everyone else, this means that a sense capacitor C_{sense} is placed between the ferroelectric capacitor and ground. The sense capacitor collects the charge from the ferroelectric capacitor, forcing the voltage on the base of T1 to equal

$$V_{base} = Q_{fe} \text{ x } C_{sense}.$$

The value of C_{sense} is chosen so that if the ferroelectric capacitor does not switch, the total charge that comes out of the ferroelectric capacitor is such that the base voltage remains well below threshold voltage of T1. Switching charge from the DOWN state, on the other hand, should cause the base voltage to rise above the threshold of T1 and latch the circuit low, just as does the circuit in the bipolar circuit of Figure 13 without the sense capacitor.

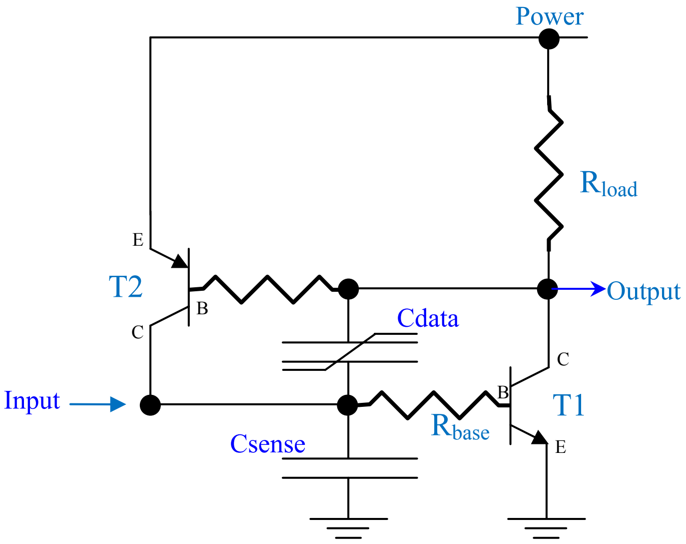


Figure 17: Charge-based state sensing circuit.

The size of C_{sense} is determined by how much charge is generated by C_{data}. The full hysteresis loop of Figure 6 is not sufficient to make this determination. Instead, half-hysteresis loops of the capacitor should be measured. The half-hysteresis loop is actually what happens to the capacitor during the read operation in the latch.

The relative amounts of charge that leave a typical ferroelectric capacitor for the switching and non-switching states when the half-loop is executed are shown in Figure 18.

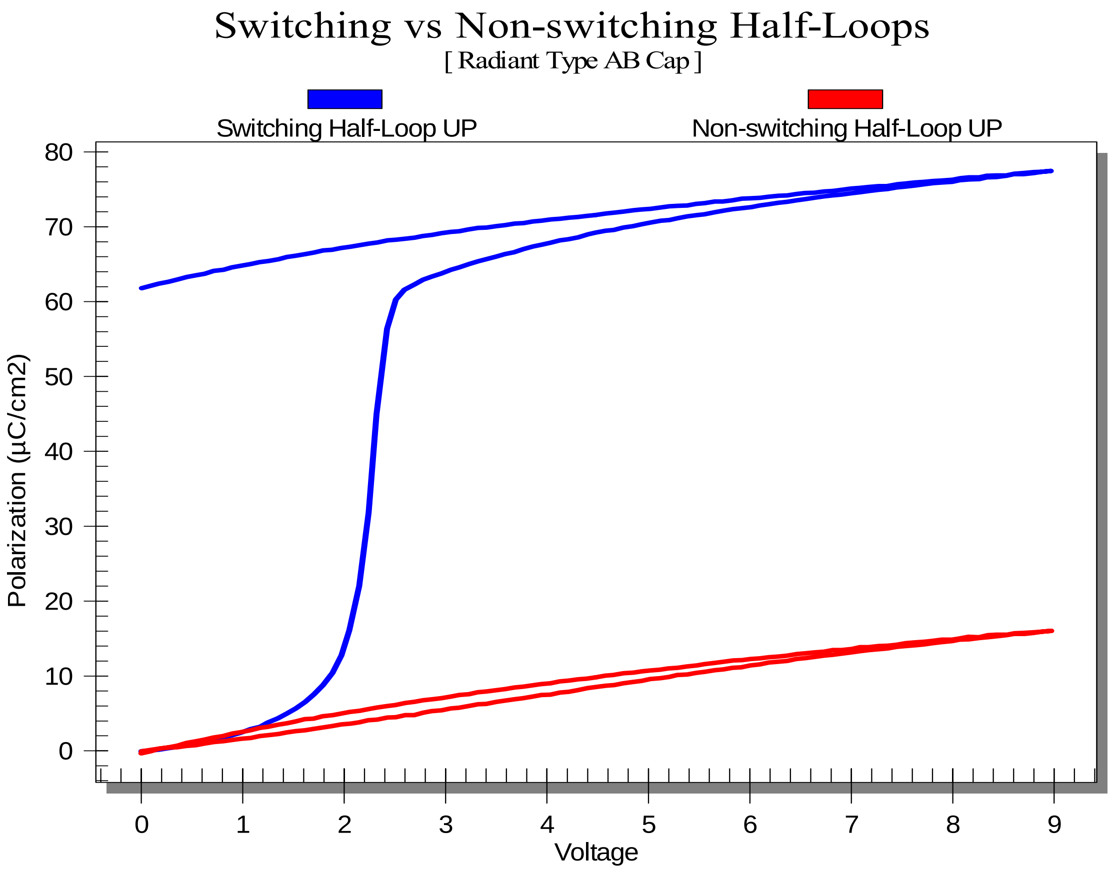


Figure 18: Switching and non-switching charge from a ferroelectric capacitor.

The two loops in Figure 18 were measured by the following sequence of voltages:

1. Negative voltage DOWN half -loop.
2. Positive voltage UP half- loop. (switching) [plotted in **BLUE**.]
3. Positive voltage UP half- loop. (non-switching) [plotted in **RED**.]
4.

A half-loop measurement goes from zero volts to the target voltage and back to zero without going to the voltage of the opposite sign. In the sequence above, the first negative voltage places the ferroelectric capacitor in the DOWN state relative to the test equipment. The first positive voltage half-loop causes switching so it represents the charge measured from the DOWN state. The first positive half-loop leaves the capacitor in the UP state. The second positive voltage half-loop then measures the charge generated from the non-switching condition, representing the UP state.

> Note that the Y-axis of Figure 18 is given in units of microcoulombs *per square centimeter* or charge per unit area. The loop in Figure 6 is plotted in units of charge. The difference is that for Figure 17, the charge generated by the capacitor was divided *by the area of the capacitor* before being plotted. The "charge per unit area" is called the *polarization* of the capacitor, hence the label of the vertical axis of Figure 18. The polarization performance of all capacitors of the same type and thickness is *independent of the area of the capacitor*. Therefore, the plot in Figure 18

can be used to predict the amount of charge that would be generated by any ferroelectric capacitor of the same type and thickness. For instance, the capacitors measured in Figures 6 and 18 were of type Radiant Type AB WHITE. These capacitors have 2600Å of 20/80 PZT between platinum electrodes. The WHITE designation means the capacitor had an area of 0.0001 square centimeters. By multiplying the values in Figure 18 by 0.0001, the values in Figure 6 can be calculated. The Type AB family capacitors have a variety of areas (color designations). Figure 18 can be used to determine the charge that would be generated by any Type AB capacitor once the area of that capacitor is known.

In the circuit of Figure 17, the charge from the ferroelectric capacitor is collected by C_{sense}. The sense capacitor generates a voltage linearly related to the total charge it contains. Consequently, the voltage on C_{sense} during a read operation will look like the charge profiles in Figure 18 for the two data states. By carefully selecting the value of C_{Sense} with respect to the area of the ferroelectric capacitor C_{data}, the voltage generated by the UP state should not be enough to turn on transistor T1 but the voltage generated on C_{sense} by the DOWN state should.

For instance, at 7V, the Type AB capacitor generates approximately $70\mu C/cm^2$ when starting from the **DOWN** condition but only $14\mu C/cm^2$ if starting from the **UP** condition. The absolute charge that a WHITE capacitor would generate would be

DOWN $70\mu C/cm^2 * 1x10^{-4} cm^2 = 7x10^{-9} C = 7nC$
UP $14\mu C/cm^2 * 1x10^{-4} cm^2 = 7x10^{-9} C = 1.4nC$

Choose the value of C_{sense} in Figure 16 for the DOWN state to turn on T1 but the UP state cannot.

C_{sense} = 10nF
DOWN 7nC/10nF = 0.7V
UP 1.4nC/10nF = 0.14V
C_{sense} = 5nF
DOWN 7nC/5nF = 1.4V
UP 1.4nC/5nF = 0.28V

The C_{sense} value can actually have a range of values in a functional circuit.

NOTE: The description for half-loop measurements does not describe the negative going loops. They can certainly be added. Or, the sample can by physically reversed! It is important to realize that polarization in a ferroelectric capacitor has a vector fixed relative to the capacitor electrodes, i.e. it points to one or the other. Physically reversing the orientation of the capacitor in the circuit, i.e. taking it out, turning it around, and putting it back in, *also physically reverses the direction of the polarization vector relative to the external circuitry and thus reverses the stored data!*

With charge-based sensing, the current flow through R_{sense} does not determine if the circuit latches as it does in the bipolar circuit of Figure 12. The value of C_{sense} becomes the controlling parameter for latching, allowing a wider range of power voltage rise times.

Memory circuits built with FETs in place of bipolar transistors must use the charge-based sensing.

Rising Edge Read Circuit

A third method of reading the state of the ferroelectric capacitor replaces C_{sense} in the circuit of Figure 17 with an $R_{threshold}$. The current through $R_{threshold}$ from the ferroelectric capacitor determines the voltage base or gate circuit during power-up. $R_{threshold}$ is sized so that the **UP** state does not generate enough current to cause the voltage on the common node between C_{data} and $R_{threshold}$ to exceed the threshold voltage of T1 while a **DOWN** state will. This particular method of reading the state of C_{data} will be very sensitive to the slope of the power voltage as it rises.

Power Ramp

In all of the circuits above, the read operation during power up is sensitive to the rate at which the power voltage rises when it is turned on *since the power line is also the read-enable line!* Power applied to the circuit automatically reads the state of the ferroelectric capacitor and restores the original state that existed before power-up. When operated from a system with inductive components or switch bounce, power conditioning may be necessary to block out bounces.

The power conditioner necessary for one of these circuits must accomplish two objectives:

1. Not power the circuit until the system power is stable.
2. Convert the external power to a known ramp rate targeted at the RC time constant of the ferroelectric capacitor in the latch.

The circuit below accomplishes both objectives:

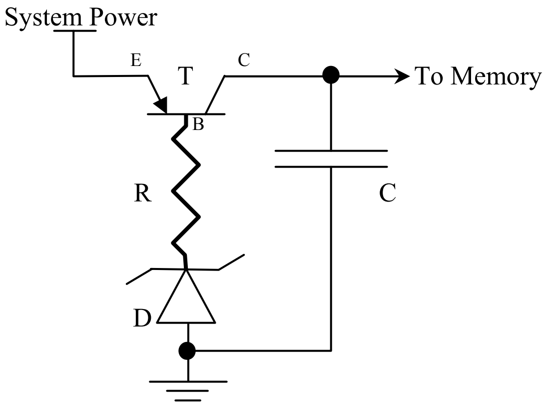


Figure 19: Power conditioning circuit for autonomous memory.

For proper latch operation, the RC time constant of the ferroelectric capacitor in the non-switching state of an aNV latch must be faster than the rise time of the power. The circuit above converts the rise time of the System Power to that acceptable to the latch. As system power rises, transistor T remains off until the voltage across Zener diode D exceeds its turn-on value. After diode D begins to conduct, current flows through the emitter-to-base circuit of transistor T. β times that base current flows from the emitter to the collector and into timing capacitor C. Base resistor R limits the I_{BE} to a constant amount meaning that the current through the transistor to capacitor C will be constant. A constant current into capacitor C will cause a constant voltage ramp across capacitor C and into the memory circuit until the voltage on C reaches the value of System Power.

Sample Circuits

Bipolar

A successful circuit implementation for bipolar components is given below along with recommended component values. The power for this configuration comes from a 9V battery. For lower-voltage batteries, reduce the value of the Zener diode in the power conditioning circuit. To make the circuit stabilize faster, use a smaller C_{data}. To withstand static discharge or power spikes that might change the data in C_{data}, use a larger value for C_{data}. Other components in the circuit must change to compensate for changes in the area of C_{data}.

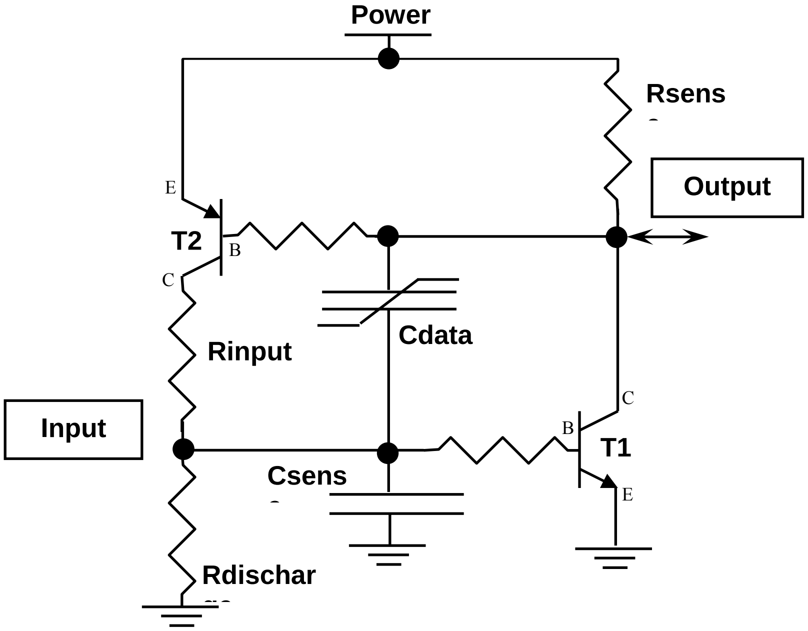


Figure 20: Example bipolar autonomous NV latch with component values.

Power Conditioning Circuit:

a.	R	22kΩ
b.	C	100nF
c.	D_z	5.1V

NOTE: These values will give a rise time of approximately 60µs for a transistor β of 80.

NV Latch:

a.	R_{Sense}	1kΩ
b.	C_{data}	Type AB WHITE
c.	C_{sense}	5nF
d.	$R_{discharge}$	10MΩ
e.	R_{input}	1kΩ
f.	PNP base R	47kΩ
g.	NPN base R	10kΩ

Sample Unipolar Circuit

If only one type of transistor is available, for instance only NPN or enhancement FETs, an autonomous latch may be constructed by adding a few more components. The circuit is below:

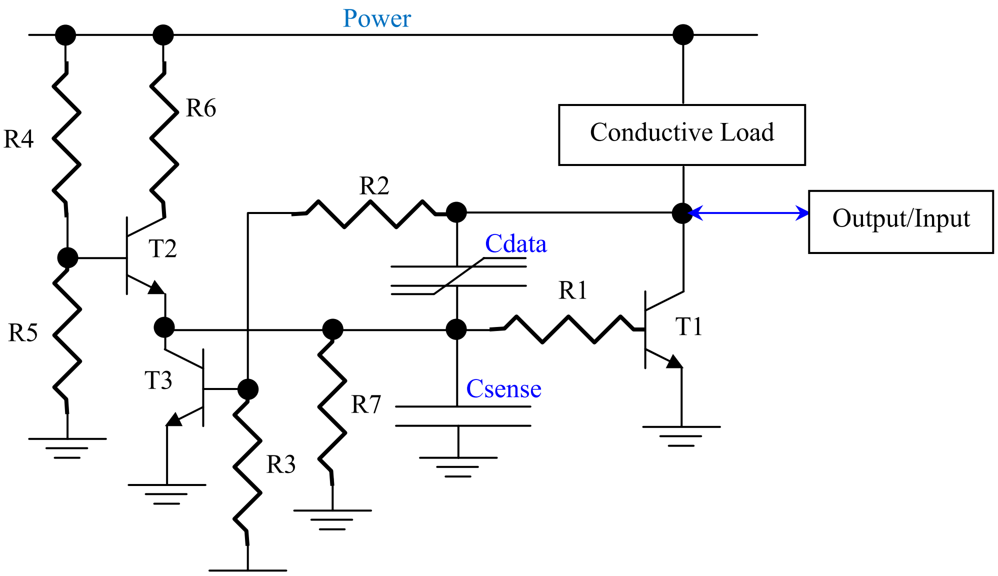


Figure 21: Autonomous NV Latch constructed with unipolar transistors.

Ferroelectric Capacitor:	1200Å 4/20/80 PNZT with an area of 10,000μ^2.
Csense:	10nF
T1, T2, T3:	2N4401 NPN bipolar transistor
Conductive Load:	100kΩ
R1:	10kΩ
R2:	417kΩ
R3:	100kΩ
R4:	5MΩ
R5:	2.5MΩ
R6:	1kΩ
R7:	50MΩ

This circuit replaces T2 of Figure 19 with the T2/T3 complex of Figure 21. The power voltages at which T3 and T2 turn on individually are determined by R4/R5 and R2/R3 respectively. T2 and T3 are cross coupled so that once T2 is on T3 cannot turn on and vice versa. T3 is turned on by the voltage at the Output. T2 turns on once System Power has reached a specific value unless T3 has already turned on.

Select the values of these two voltage dividers to meet the following two conditions:

1. T2 must turn on at a Power voltage *higher* than does T3.

2. The Output voltage at which T3 turns on must be *above the shelf voltage*.

If the shelf voltage does not occur, T3 turns on before T2 turns on as Power keeps rising. This latches the UP state by preventing T1 from ever turning on. If the shelf voltage does occur, T3 cannot turn on while the shelf voltage exists. T3 is held off until Power gets high enough to turn on T2, latching the circuit into the DOWN state by forcing T1 on.

> NOTE: The component values listed above for the circuit in Figure 2 were used to make a functional autonomous latch using only one transistor type. The resistor values listed may not be optimal. For instance, the R4/R5 voltage divider has very large values limiting the base current of T2 to a very low value and thus limiting the current through T1. R4 and R5 could be reduced by a factor of 10 and the circuit should still work.

Type AL Capacitor with LSCO electrodes

Adding Perovskite electrodes to the PZT capacitor gives it almost zero fatigue and zero imprint. At Radiant we use Lanthanum Strontium Cobalt Oxide electrodes for this purpose. Other organizations successfully use Strontium Ruthenium Oxide electrodes or Iridium Oxide electrodes. LSCO-based capacitors switch more slowly than do the Type AB capacitors with their metallic platinum electrodes. A Type AB capacitor will give the polarizations shown in Figure 18 independent of the read speed into the hundreds of nanoseconds. Type AL capacitors will give the polarizations shown in figure 18 at 100 milliseconds or slower. The remanent polarizations will decrease about 12% per decade as read speed increases. Thus, a read operation at 100µs will generate approximately 36% less switching charge than a read operation at 100ms. For reliable operation with a larger switching signal for Type AL capacitors with LSCO electrodes, R in the power conditioning circuit should be increased to 220kΩ to slow the power rise time by a factor of 10 or 2.2MΩ to slow the rise time by a factor of 100. Otherwise, the circuit values should be the same.

Discharge Resistor

The discharge resistor in Figure 19 discharges C_{sense} to prepare for the next read operation. The sense capacitor will discharge through the base circuit of T1 as well. If power-up/down occurs less frequently than T1 discharges C_{sense}, no discharge resistor is necessary for safe operation. If a FET is used for T1, then a discharge resistor or discharge circuit of some type must be used to ensure that C_{sense} has no charge on it when the next read cycle takes place.

Output Stages

The autonomous memory is best used driving more powerful circuits. This is easily accomplished by driving the V_{Output} of the circuit in Figure 19 into the base of a larger NPN transistor, known as an "open-collector" logic output. The user attaches the external circuits to be controlled to the collector of the NPN transistor. If this is done, the base resistance of the power NPN transistor determines how much current is drawn through R_{sense} when the NPN transistor is turned on. Care must be taken to ensure that the current leakage through base resistor of the external power transistor during power up does not bias R_{sense} so that the voltage drop across it always exceeds 0.7V independent of the state of C_{data}. If this happens, replace the NPN transistor with a FET or use a high value base resistor for the NPN power transistor. For instance, for the circuit component values given for Figure 19 above, the base resistor of the external NPN transistor attached to the memory output node in Figure 22 must be 100kΩ or higher.

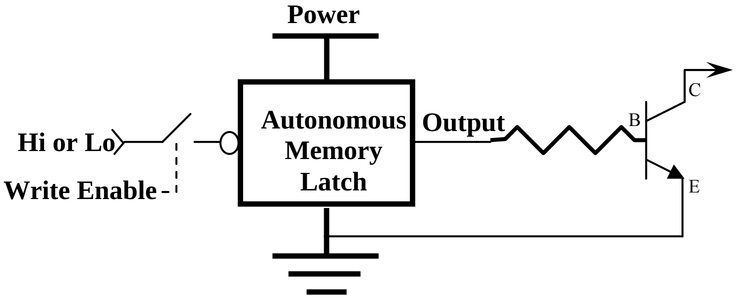


Figure 22: High impedance inputs.

No-Power Writes

An interesting property of the circuit in Figure 13 is that *it may be written with the power off!* Thus, the ferroelectric capacitor could be used to detect a change in state for an external object *while power to the circuit is off.* The state of the ferroelectric capacitor will then be latched by the circuit on the next power cycle.

Moderate Output Impedance

As mentioned at the beginning of this application note, the true memory bit should have only three connections: power, ground, and a single I/O. The one I/O line acts as both output and input because the external circuitry simply pulls the output to the desired state and it remains there even after power has been removed and returned. For the circuit in Figure 20, the outside circuit attempting to set the Output must be able to deliver more current that the memory circuit can generate in the two states. If the Output is high, the external driver must pull it down to ground against 1000Ω, relatively easy for any logic circuit. If the Output is low, however, the external driver must pull the Output high against transistor T1 while the transistor is conducting. This can be accomplished if the value of R_{base} for both transistors is adjusted to allow a low conduction through T1 while it is latched DOWN. The external driver 1) must be able to generate more current than the maximum T1 will conduct and 2) must be able to pull the Output to within Vth of Power to turn off T2. If the external driver meets these conditions, the circuit in Figure 20 may be operated as a three terminal memory bit.

MOS Considerations

The autonomous memory circuit in Figure 20 may be replicated with discrete MOS transistors. The autonomous NV circuits may also be transferred to integrated circuit processes that already support embedded ferroelectric capacitors. The latches may be placed throughout a chip to save and recall local logic levels on power-up, turning any logic circuit into a CPLD without the floating gate or flash transistors.

The circuits of Figure 19 and Figure 20 can be replicated with MOS transistors in place of the bipolar transistors in a CMOS process. Resistors, easily implemented in discrete form, are more difficult in a CMOS process. They can be replaced by MOS transistors with fixed gate voltages that bias the transistor conduction into the ohmic region of operation.

The circuit in Figure 13 becomes an all-CMOS based circuit in Figure 23.

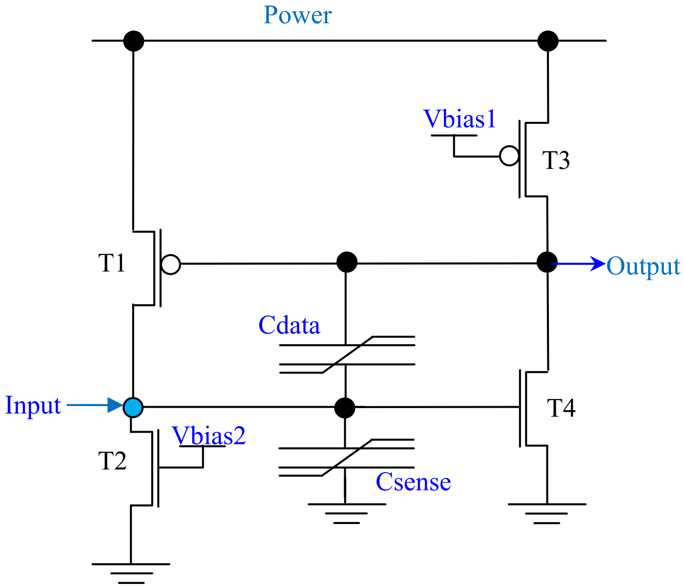


Figure 23: Autonomous NV Latch constructed with CMOS transistors.

T2 is a necessary addition to discharge C_{sense}. Otherwise, there is no discharge path for C_{sense} since most nodes in CMOS are extremely high impedance. The circuit cannot be turned off and turned on again any faster than the discharge time of C_{sense}. The RC time constant for T2 and C_{sense} must be much longer than the settle time for the circuit during power up. As well, T2 in this configuration must not be able to overpower T1 when T1 is on. The "resistor" in the T2 position of Figure 23 may be replaced with a low value constant current source or an n-channel transistor configured as a reverse-biased diode.

C_{sense} itself can be constructed from another ferroelectric capacitor to save space. The voltage across it from the gate to ground will always be positive so it will always operate as a non-switching, slightly non-linear capacitor. Careful analysis of Figure 18 indicates that it will probably have to be 20 to 40 times larger than C_{data} in area to act as a sense capacitor. An example of this calculation is provided below:

Switching polarization expected from C_{data} = $70\mu C/cm^2$

Capacitor area = $1\mu^2$ = $1x10^{-8}cm^2$

Switching charge expected from C_{data} = 0.7pC

Detection voltage for T4 = 0.7V at **0.35pC** on C_{sense}

From Figure 18, non-switching polarization at 0.7V = $2\mu C/cm^2$

Capacitor area required to generate 0.7V at 0.35pC = $0.35pC/2\mu C/cm^2$ = $17.5\mu^2$.

Note that this example set the high detection state at 0.35pC instead of the fully saturated 0.70pC. The size of the sense capacitor is dictated by the product definition.

There is a capacitance associated with the gate and source of T4 in Figure 23. This capacitance is in parallel with $C_{sense.}$ For the example circuits given in this application note, C_{data} is a Type AB WHITE ferroelectric capacitor with an area of 10,000 square microns, requiring C_{sense} to have values between 5nF and 10nF. Any gate capacitance T4 might have will not affect this circuit. On the other hand, this circuit can be made to be very fast or sensitive to very small outside write power by making C_{data} very small. A Type AB capacitor with an area of 10 square microns has an equivalent capacitance of roughly 1pF. Typical ferroelectric capacitors in existing CMOS processes are again much smaller than $10\mu^2$. Given such a small C_{data}, the parasitic gate capacitance of T4 may be enough so that an external discrete C_{sense} might not be necessary.

IC Design

This section considers the use of the autonomous memory circuit as individual bits distributed throughout a logic circuit or IC. In this situation, the product definition may require each bit to be totally autonomous from external control. Or the product definition may allow global control of certain functions of the memory, essentially creating semi-autonomous memory operation as opposed to autonomous operation. Semi-autonomous operation may allow for smaller bit areas, a key goal in IC. The advantage of sending control signals generated by the IC to autonomous bits on the IC is that a single control line may be all that is needed to control all bits on the chip. For instance, the autonomous bits may not be allowed to execute a read operation until Vcc inside the chip has been stabilized by the on-board power regulation circuitry.

Another unique characteristic of the autonomous memory is its technology independence. Normally, memories are built in CMOS technology because of real estate, power consumption, and density advantages. The autonomous memory circuit allows small non-volatile memories to be built on bipolar or biCMOS process lines. Bipolar circuits are particularly resistance to radiation damage in the outer space environment, leading to the possibility of radiation-hard non-volatile space-qualified bipolar ICs.

CMOS circuit design in an IC leads to unique problems that are easily solved in the discrete circuits described earlier. The discussion below explores these problems.

The traditional four-transistor CMOS latch is difficult to implement as an autonomous memory. See Figure 24 below. The problem is that the gate of T2 is connected to the Output so that when power is applied T2 becomes conductive ($V_g = V_{Output} \sim 0.7V$) before C_{data} reaches its coercive voltage and begins to switching if it is in the DOWN state. In a balanced CMOS latch circuit where all transistors are of the same dimensions, T2 will discharge C_{sense} much faster than T3 will charge it. Despite this problem, T2 or some circuit replacing T2 must be used at that node to discharge C_{sense} *after the memory has settled into its memory state after power up*. Otherwise, with Output high and T1off, the C_{sense} node will be floating against super high impedance paths to ground. C_{sense} would take a very long time to discharge. Additionally, any disturb, such as an alpha particle hit to that floating node, might activate T4 and cause the latch to switch states. Therefore, the C_{sense} node must be held at ground *after* the high output state is established. Whatever mechanism is used to reproduce the function of T2, *it must not engage* while the read is taking place or it must be so weak that it will not cause an error in the read operation.

> Note: Functional thin ferroelectric film capacitors are getting thinner as researchers make progress, lowering their switching voltage. In the future, once a ferroelectric capacitor can be fully switched at a voltage below the MOS threshold voltage, a traditional four-transistor CMOS latch may be used.

One solution to this problem is to reduce the current capability of the T2 circuit leg to the point that it cannot affect the read operation. The circuit in Figure 23 solved this issue by forcing T2 to operate as a high value resistor. A second approach is to give T2 a geometry relative to the other three transistors plus the value of C_{sense} such that T2 cannot discharge C_{sense} fast enough to affect the accuracy of the read operation during power-up. Alternatively, T2 could be configured as a reverse biased diode. Its reverse biased diode current could not be allowed to overpower T1 or the read operation but would eventually discharge the C_{sense} node if that node is floating. A fourth approach would be to replace T2 with a low value current source that would constantly discharge C_{sense} at a very slow rate.

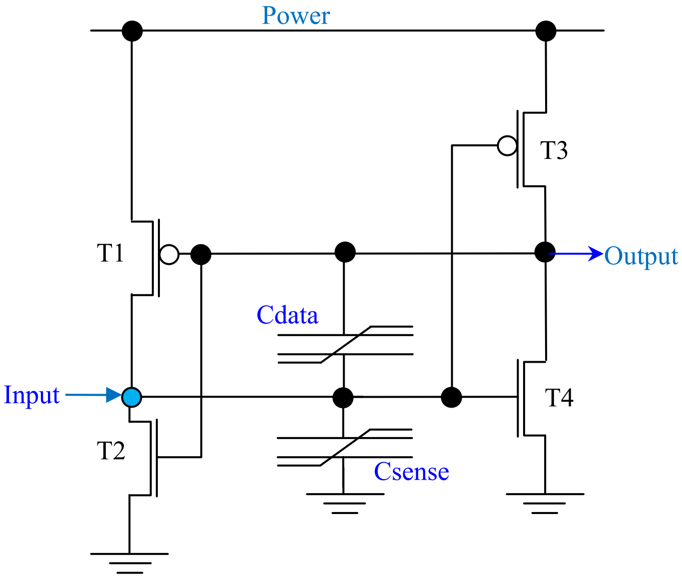


Figure 24: Asymmetrical Autonomous NV Latch constructed with CMOS transistors.

To more powerfully clamp the circuit in the high state to prevent single-event-upsets, a higher current switch must be used in the T2 leg. Such a switch must

1) not turn on unless the memory output is high and

2) not turn on until the read operation is safely completed.

The second requirement can be met locally by using a comparator to determine when power to the memory has exceeded the saturated switching voltage of the ferroelectric capacitor or by using a "power-on reset circuit" that determines when power is stable before providing a "data valid" signal to the circuit. The output of such the decision circuit must be ANDed with the memory output in order to meet condition one above. The AND function may be most easily accomplished by adding a second n-channel transistor to the T2 leg, transistor T2a. T2a is controlled by the local decision circuit or, in semi-autonomous operation, by a global enable generated by the chip. See Figure 25.

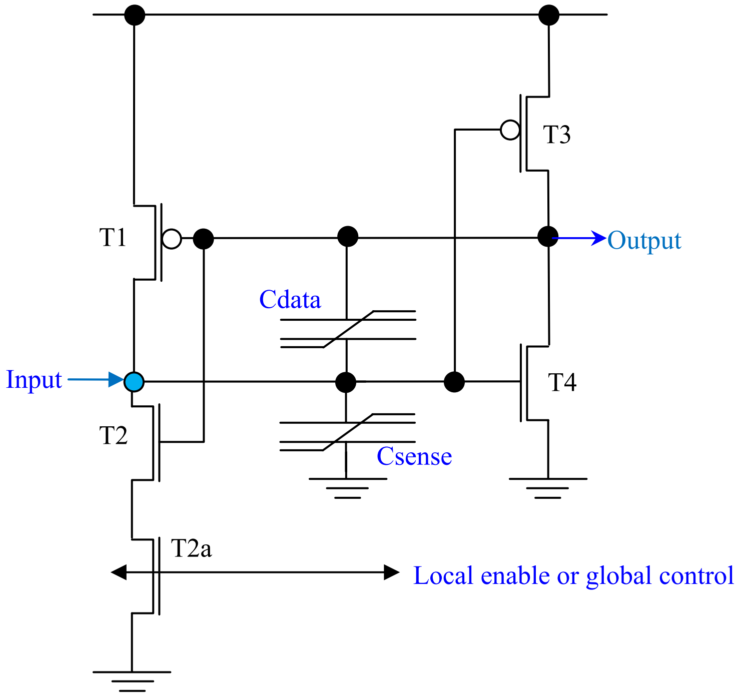


Figure 25: Asymmetrical Autonomous NV Latch constructed with CMOS transistors.

Power conditioning for the CMOS or NMOS autonomous memory circuits may or may not be needed. Many ICs already have internal power conditioning for sensitive components inside the chip and that conditioning may be enough to prevent improper read operation by the autonomous memory circuits. On the other hand, the designer might use a global control line and p-channel transistors to isolate the autonomous memory circuits from the main power bus until the bus has stabilized. A third approach would be to create a secondary global power bus for the autonomous memory bits that meets the rise time requirements for error-free read operation of the bits. It can be enabled and disabled at a single point to allow independent application of memory circuit power isolated from the main power bus.

Acknowledgement: I would like to thank Richard Womack of Albuquerque, NM for his review and recommendations for solutions to the IC design issues discussed above.

SCR-based Memory

A close examination of the circuit in Figure 20 indicates that it has the same function as an SCR, silicon controller rectifier. An SCR is essentially a diode with a third control line. It is normally off with a voltage applied across it until a signal on the control line turns it on. It will remain on until power is removed from its diode path. An SCR has a P/N/P/N stack. The path from Power through the PNP transistor and the base of the NPN transistors in Figure 20 has a P/N/P/P/N stack. It is possible to build an "Autonomous SCR" using IC fabrication technology.

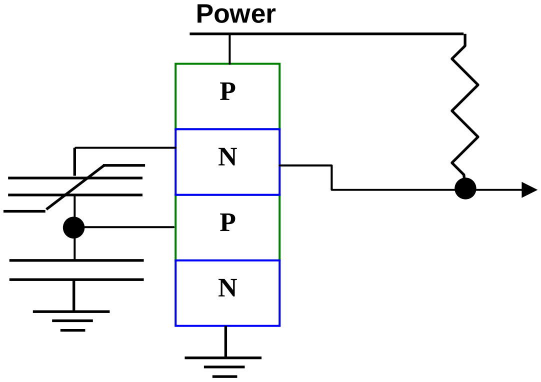
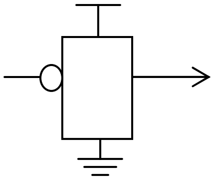


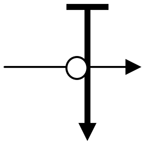
Figure 26: A non-volatile SCR circuit.

Nonvolatile Logic Lines

The autonomous memory latch is useful in four formats described below. The single memory bit is not a new concept but using the autonomous latch it can be implemented with a minimal component count and no clock circuits. The other three concepts are new and offer the possibility to implement circuits and electromechanical systems with intrinsic memory. The in-line NV inverter and buffer can be added to an existing logic design to make *logic lines non-volatile*. The non-volatile switch allows relays, control circuits, motors, etc. to remember their last state. Envision a factory as a CPLD!

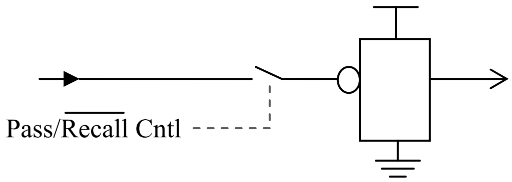
Standalone Memory Latch:

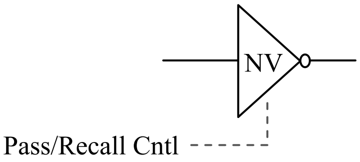




There is a bubble on the input to the latch because the output of the latch takes on the opposite value of any signal applied to its input. The input can be driven by a 3-state line such as the output of a microprocessor or a buffer. The output of the latch can drive the input to any logic device with input impedance higher than the output impedance of the latch.

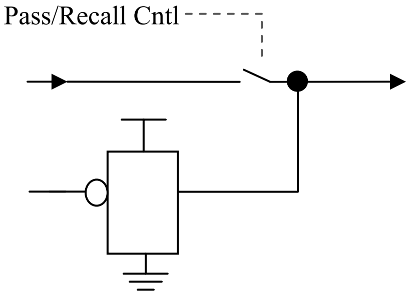
In-line NV Inverter:

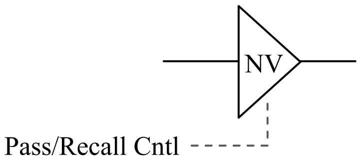




This circuit is inserted into a logic line as an inverter. With the switch closed, it acts as an inverter. With the switch open, the latch will hold the last state as a memory bit and will recall that state on power up. In order to securely recall a logic state on power-up, the switch should be opened prior to power down to prevent random noise generated on the logic line from affecting the latch state as the logic powers down. The switch should remain open after power up until the logic controlled by the memory bit has stabilized. It is very important to note that this tristate control *is on the input of the circuit.* Tristate controls in traditional logic circuits *are on the output*.

Parallel In-line NV Buffer:

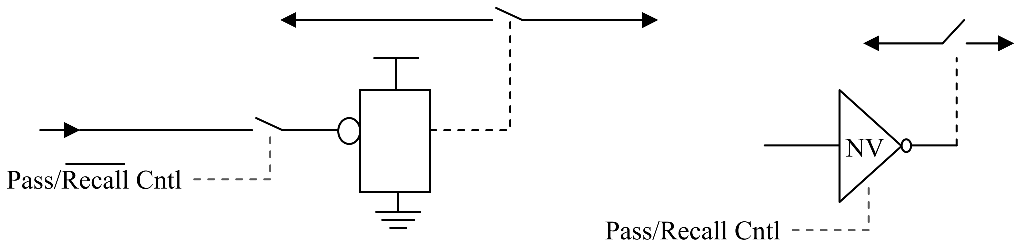




This circuit is the non-inverting buffer version of the inverter above. Using a moderate impedance output version of the autonomous latch, the latch state will follow the logic signal it is connected to if the switch is closed or hold the last value written before the switch opened. Like the inverter, this circuit will recall the last stored state on power up. Since this circuit has moderate output impedance, it must drive a high impedance input. The input line is left unconnected. Or, it can be connected to other circuitry as a separate input to the logic line.

This function may also be accomplished using the In-Line NV Inverter with another inverter on its output.

NV Switch:



This circuit is a non-volatile, programmable analog switch. The upper switch can be a high current analog switch or relay to control much more powerful circuitry.

Higher Level Complexity

The latches may be combined into a higher level of complexity such as registers and counters. Registers formed from these latches may be placed in any system and used anywhere, especially systems that have intermittent power. Such systems could be remote sensors powered environmentally, an RF-powered smart card with no battery, or even a smart credit card with a built-in human-operated power source that would allow the user to change his or her PIN at will *without the need of an external reader/writer like an ATM.*

Non-volatile counters built with autonomous memory bits offer a unique opportunity to create autonomous sensors. Already described above is the use of a single latch as an event detector while un-powered. Digital counters combining multiple latches, one for each bit, where the entire circuit is powered intermittently by an environmental event *become environmental Analog-to-Digital Converters*. Such a circuit would be powered from the counter input. When powered from the counter input, the counter will advance one count for each event. Or, when powered from the input the counter might advance multiple counts according to an internal timer, thus mapping the total time power is applied. In either case, when powered from a separate power pin by a controlling circuit or an RF signal, the circuit does not advance but instead reports its count. After being reset back to zero, the counter is ready to measure new activity on its count input. Examples are given below.

Attach a digital counter to a generator attached to a water wheel in a water supply pipe. When water flows in the pipe, it generates power for the counter which is calibrated so that its count rate when powered matches the water flow. When water is not flowing, the counter retains its historical value. The count can be read remotely by the water utility as is done today with battery powered meters.

In a different situation, the counter may be powered by a solar cell, thus recording the total solar flux at that location. Multiple counters can be utilized to differentiate between hours, days, weeks, or months. In fact, any environmental effect from radiation, solar flux, wind, water flow, or earthquakes may power a counter or counters and be *measured* remotely and autonomously by an autonomous memory circuit. In this way, the counter is an autonomous ADC measuring the energy flux of the external power source.

Radiant has already released several public white papers about this subject. See “An autonomous nonvolatile digital counter.pdf” and ”An autonomous NV counter for radiation environments.pdf” from Radiant.

Conclusion

The autonomous non-volatile latch architecture allows functional memory bits to be constructed from discrete components or added to integrated circuits. A wide variety of circuit configurations are possible in order to meet different applications. This application note described the fundamental theory and operation of the autonomous memory and then provided example circuits with component values. Implementing autonomous memory into logic circuits, controllers, or industrial equipment enables new and unique architectures for ICs, controllers, or factories. For more background about ferroelectric capacitors and how they work, go to Radiant’s web site at www.ferrodevices.com and download the documentation for the Radiant EDU educational tester. The documentation has several chapters giving simple explanations of the internal workings of these incredible components.