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Cascading Individual Analog Counters

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Introduction

It is possible using Radiant's ferroelectric Event Detector circuit to store analog memory values or count events in a single ferroelectric capacitor. Although ferroelectric capacitors have a huge number of possible intermediate states in their remanent polarization, the ability of some circuits to determine that polarization state precisely during a read or write operation is limited by the sliding of the hysteresis loop left and right on the X-axis. That slide changes the voltage at which remanent polarization states occur in the capacitor but not the amount of remanent polarization itself. A system that combines circuits that meter charge into the capacitor (a charge source) combined with an accurate charge counter (electrometer) that measures the charge inside the capacitor exactly can discriminate a large number of states. These types of circuits can be implemented on IC dice with the analog circuits and ferroelectric capacitors but they are not efficient in area or parts-count to use for discrete circuits with packaged ferroelectric capacitors. Autonomous Event Detector circuits can easily be implemented using discrete components but charge sources and electrometers require a lot of power and a lot of space when constructed discretely. A more elegant approach for discrete memory is to connect the analog circuit to a low power, low pin count microprocessor that writes and reads analog states in a single ferroelectric capacitor using pulses or timed voltage applications. These two approaches will be limited to a total of five to 16 states in the capacitor depending upon the quality of the ferroelectric capacitor. To count higher, such low-count circuits can be cascaded much in the way that binary counters are constructed. The difference with binary circuits is the need to reset the ferroelectric capacitor back to its zero count when its count rolls over. Cascading analog counter circuits for large number counts is the subject of this document.

Why count with a ferroelectric capacitor?

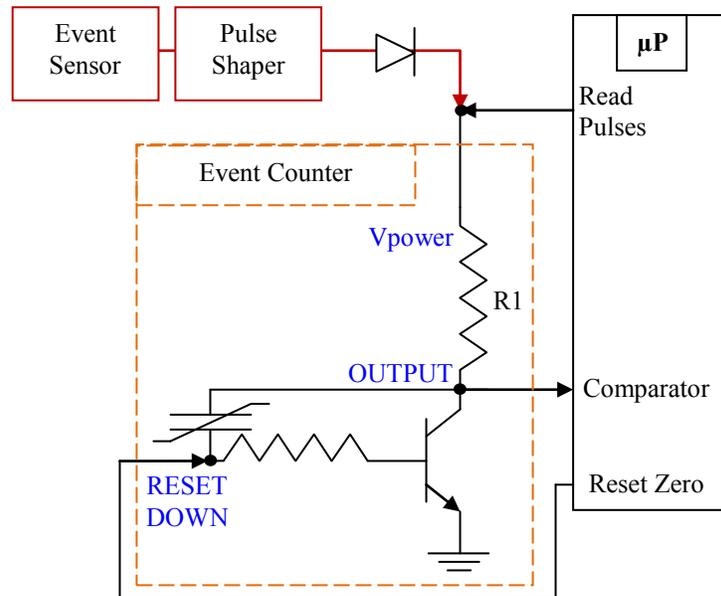
Why use a ferroelectric capacitor to count pulses or events when the same thing can be done with an off-the-shelf microprocessor? The reason is power demand. A ferroelectric counter can be constructed using small area ferroelectric capacitors that can be written by an environmental sensor with as little as 30nJ in 30 microseconds for a PZT capacitor having an area of 100 μm^2 operating at 5 volts. PZT capacitors can be made even smaller and operate at lower voltages. Such small spurts of energy are not enough to power up a microprocessor long enough for it to

boot, recall the count, increment the count, store the new count, and shut down but it is enough to change the analog count of a ferroelectric capacitor.

Even if the ferroelectric analog event detector can only count reliably to 5, cascading 6 counters will yield a maximum count of 15000, enough to count the total steps for a 10-mile run using a sensor buried in the runner's shoe. A marathon requires a count of perhaps 35,000 steps which can be handled by cascading 6 ferroelectric counters that each count to 6. As ferroelectric capacitor quality improves with time and manufacturing experience, they will be substituted into existing counter circuits to raise the count limits.

To cascade analog counters requires extra energy to run the glue logic. From the example above of 30nJ for a single bit in a 100 μm^2 ferroelectric capacitor, each count stage at worst case will require the energy of one pulse. For six stages, that is 180nJ. Add to that the energy required to power and operate the glue logic connecting the stages. Assume for now that the glue logic for each stage requires 10 milliwatt for 10 microseconds to perform its operation. That amounts to 100nJ per stage or 600nJ. Combined with the 180nJ in energy required to move the remanent polarization in the ferroelectric capacitors indicates that each count for a six stage ferroelectric analog counter needs less than 1 μJ per count worst case. This level of energy is easily available from a piezoelectric energy harvester in the sole of the shoe or the sleeve of a shirt or some other human energized activity.

A single capacitor counting circuit with a microprocessor as a controller is shown below. The unique advantage of the microcontroller is that its I/Os can be set to HiZ during low energy counting so its inputs do not load the memory circuit or the event sensor.



Note that the microprocessor required to read and reset the counter is not powered up during counting so *it does not use energy while counting*.

Theory

Radiant has several documents placed on-line describing the theory of autonomous ferroelectric memory and its use as a digital or analog memory element. The details of the theory will not be discussed here. Please see the following documents at

http://www.ferrodevices.com/1/297/application_notes.asp

“Exploring Autonomous Memory Circuit Operation.pdf”

“Autonomous Analog Memory.pdf”

“Operating an Analog Event Detector.pdf”

Read the document “[Primer for Autonomous Memory Design.pdf](#)” for a detailed circuit analysis and design tips.

Cascaded Counters

For all four possible operating methods of the autonomous memory circuit

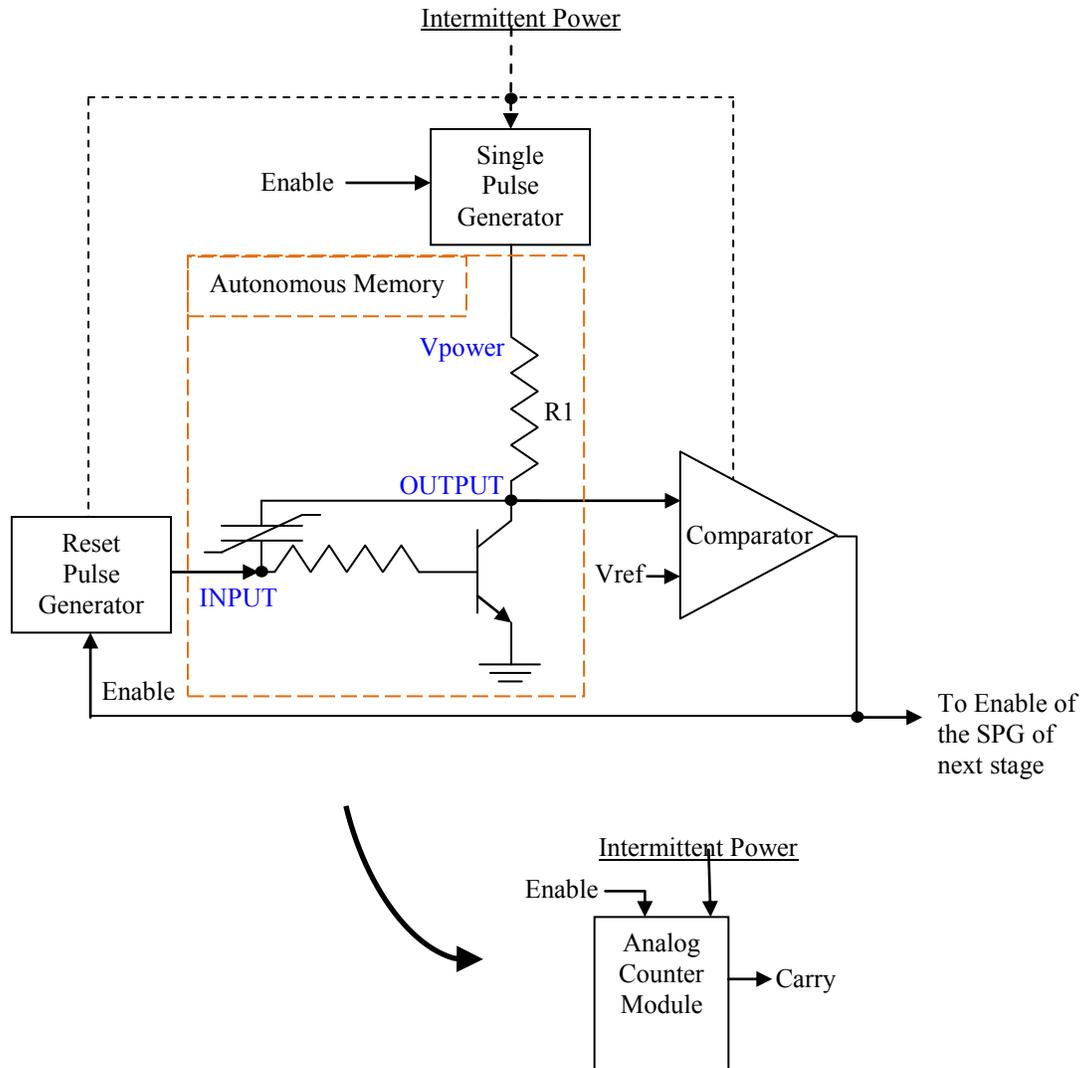
1. Preset DOWN -Write UP – Read UP
2. Preset DOWN -Write UP – Read DOWN
3. Preset UP - Write DOWN – Read UP
4. Preset UP - Write DOWN – Read DOWN

the detection of the *saturated state representing zero* is the same: A voltage threshold is detected on the OUTPUT and read by the controller. That voltage may be positive or negative depending upon how the circuit is constructed and operated. The threshold can be detected by a comparator circuit so no extra intelligence is necessary to tell when a counter has reached its full count.

To cascade counters, three actions are necessary:

1. Detect the end of a count of a single analog counter circuit using a comparator.
2. Apply a count pulse of ‘1’ to the next counter above it in the cascade.
3. Reset the lower counter back to its starting position.

The architecture for a single stage of the cascaded counter is below.



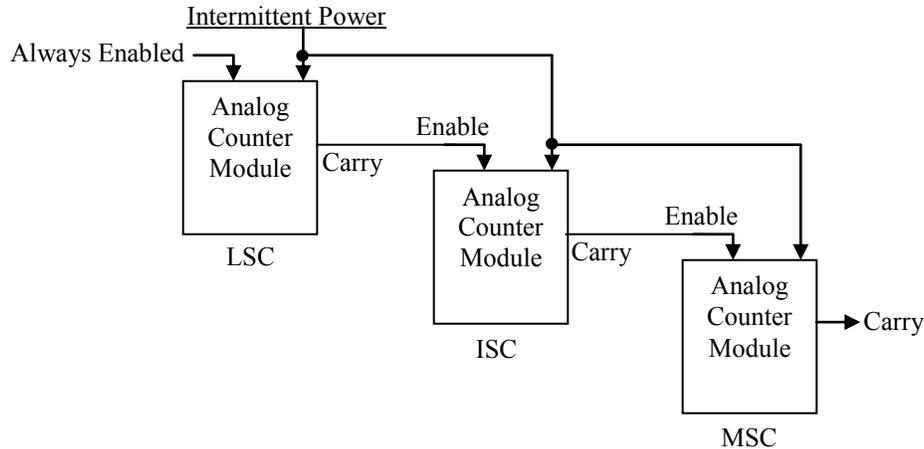
Definitions:

1. Intermittent Power: Power voltage from a controller or an energy harvester or a sensor. For counting from an external sensor, Intermittent Power must turn ON *and* OFF every time a count pulse is to be recorded. The counter increments its count by '1' only once each time Intermittent Power turns ON. Intermittent Power has two design limitations:
 - a. It must be able to power all of the components in the cascaded counter.
 - b. It must remain ON long enough for every component in the cascaded counter to complete its count and for the carry to ripple through.

2. A controller assigned to read the counter should be able to turn on the circuit and actuate the two pulse generators independently to read the count and reset the circuit to zero. These connections are not shown but are skill-of-the-art for a logic designer.
3. Single Pulse Generator on the Vpower port: The SPG generates a single voltage pulse of a fixed width which represents a single count into the Vpower port of the autonomous memory circuit every time it receives power from Intermittent Power *but only if that SPG is Enabled*.
4. Reset Pulse Generator is another SPG that applies a voltage pulse to the INPUT node of sufficient energy to set the ferroelectric capacitor full DOWN when it is Enabled. The asymmetry of the impedance from the Vpower node and the Input node ensures that reset requires far less than a microsecond.
5. Vref: the voltage from the OUTPUT of the autonomous memory that is established as representing full UP, *the full state*.

In this example of counter operation, the ferroelectric capacitor begins in full DOWN. It is set down from the INPUT port. Every time Intermittent Power turns ON and the SPG Enable is true, a sub-saturating pulse is applied by the SPG to the Vpower node to increment the ferroelectric capacitor remanent polarization one unit UP. When the ferroelectric capacitor will become *full* on the next pulse, OUTPUT will become equal to or go higher than Vref on the comparator reference input during the pulse. The comparator will fire. The output of the comparator becomes the Enable for the SPG for the next module in the cascade to force that counter to increment by '1'. The output of the comparator will also trigger the reset pulse on its own circuit's INPUT to switch the ferroelectric capacitor to full DOWN (*empty*) for the next cycle of counts. Race conditions can be avoided using edge detection on the SPG and RPG inputs. If a race condition might occur, the Reset must happen at the end of the Intermittent Power pulse so the comparator remains ON for the duration.

Cascaded counters are connected as follows:



Notes:

1. Let's say a 9-pulse counter is used as a counter with 3 binary bits (count = 8) of stable analog states. Starting with the counter at 0 at full DOWN, 8 pulses applied to the Vpower port must cause the comparator to fire, resetting the counter to zero on the 8th pulse. Executing an 8-pulse count in a counter capable of counting to 9 can be done one of several ways:
 - a. The count pulse widths can be made slightly wider to move a little more remanent polarization on each count so only 8 pulses fit in the capacitor.
 - b. The counter can be left capable of counting to 9 but Vref can be set a little lower so it fires after 8 pulses, not 9.
 - c. The 9-pulse counter could be turned into a 4-pulse counter again by setting Vref lower again.
 - d. Because ferroelectric capacitors switch steeply in a small voltage range near the coercive voltage on their hysteresis loops, the reference voltages for pulse counts in the middle of the shelf are close together. It may be more reliable to change pulse widths for shorter counts than to set a lower Vref.
2. To read the counter, a microprocessor associated with the circuit turns on the SPG of a single stage at a time and continues the count until that stage is full. The stored value in that stage is calculated as

$$\text{Stored Value} = \text{Maximum Count} - \text{Read Count}$$

For example:

- a. Suppose that a read operation from full DOWN, the zero state, requires 8 pulses to fire the comparator.

[8 max - 8 read pulses = 0 state stored in the capacitor]

- b. If 7 pulses are applied to the circuit after being set to the zero state (full DOWN), a read from that point will see the comparator fire on the first read pulse.

[8 max - 1 read pulse = 7 state stored in the capacitor]

- c. If 2 pulses are applied to the circuit after being set to the zero state (full DOWN), a read from that point will see the comparator fire on the sixth read pulse.

[8 max - 6 read pulse = 2 state stored in the capacitor]

3. Once the individual stored count of each stage is collected and calculated, the microprocessor can construct the total count by multiplying the count of each stage by its mathematical power and summing the products.
4. The last step for the controller is to reset all stages DOWN (zero at each stage) so the counter is ready for the next count.
5. Carry-look-ahead is not shown for this circuit but it could be implemented.
6. This particular example assumes that the counting state operates at minimum energy and that the read operation by the microprocessor takes place powered from an external source. Therefore, the read operation does not have an energy or time limit. It can be complex and take much longer than a single write pulse.
7. The read controller must be capable of three functions:
 - a. Powering the counter at will while isolating the counter energy source. (See **Appendix B.**)
 - b. Individually firing the SPG of each counter in the cascade individually while monitoring that counter's Carry bit to determine that counter's stored value.
 - i. This could be done in parallel for all stages of the cascade to allow determining the full count in only 8 pulses.
 - c. Firing all Reset Pulse Generators in the cascade to set "000".