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An Autonomous Nonvolatile Digital Counter

Radiant Technologies, Inc. has developed an autonomous nonvolatile memory latch capable of operating independently of a microprocessor or controller. The latch is a three-line memory cell (power, ground, and input/output) that retains its state with or without power. It uses one ferroelectric capacitor as the memory storage element. If this latch is used at each output of a classic digital counter circuit, the circuit will be able to count and to be read while operating in an intermittent power environment. A description of the circuit architecture is below. For a description of the operation of the autonomous non-volatile memory latch itself, see the document "An Autonomous Nonvolatile Memory" available from Radiant.

A binary counter may be fabricated using a variety of architectures but in the simplest implementation each digital bit is a divide-by-two flip-flop triggered by the previous bit. To allow operation in an intermittent power environment, one where continuous power is not necessary to maintain proper operation, the circuit should autonomously without external or internal clocking present its last count each time it is powered up. The autonomous ferroelectric nonvolatile latch enables that functionality.

Another approach would be to establish a standard binary counter with a parallel autonomous nonvolatile register. Each autonomous nonvolatile latch in the register follows the output of the bit it monitors, storing the output value with no need for a clock or control lines. On power up, the contents of the non-volatile latch transfers to the counter before it begins accepting count clocks. In reality, a variety of logic devices, even microcontrollers, may function under intermittent power if built with the autonomous nonvolatile latch.

Ferroelectric capacitors require little energy to switch their states and can operate as fast as nanoseconds. A thin PZT film capacitor with an area of $1\mu^2$ requires only 6pJ of energy to change its state. The latch circuit utilizes 100 times that energy, 600pJ, to execute a read. A unique feature of the autonomous counter is that the ferroelectric capacitor memory is not affected by the time period over which it is switched so the 600pJ may be applied in less than 1 micro second or for longer than a second, a characteristic that allows the system designer to control power consumption. The energy requirement for an autonomous latch is so low it may be designed such that it powers up from the clock pulse alone without having a separate power supply operating during the count. A 16-bit autonomous counter operating from 10 microsecond wide clock pulses would require only 1mW during each 10μs pulse to advance a count where all bits flip.

A unique and useful "sensor with memory" can be created with the autonomous nonvolatile counter. An external sensor that generates power as its normal function can generate clock pulses for the autonomous counter to keep track of the number of events. No power supply is necessary during the counting period. If, on the other hand, the sensor generates clock pulses at a rate *proportional* to the intensity of the event being sensed, the counter will record the total energy seen during the event. A separate power pin allows an external circuit or controller to 1) power the circuit without advancing the count, 2) read the count, 3) reset or preset a start count, and 4) unpower the circuit for it to continue autonomous unpowered operation. An array of autonomous intensity sensors where each sensor responds to a different envelope of the event being monitored enables *autonomous spectroscopy*. Using non-contact RFID technology for the controller creates more applications for remote zero-energy sensors operated using energy scavenging circuits.

A memory that operates without a microprocessor or controller eliminates complexity and enables new architectures unlike any that have been conceived before. Please contact Radiant Technologies, Inc.

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