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An Autonomous Nonvolatile Memory Latch

Ferroelectric memory circuits to date embed ferroelectric capacitors within a nest of control signals, clocks, and programming lines. This is true for both memory arrays [1, 2, 3] and latch circuits [4, 5]. This arrangement does not fully exploit the data storage properties of ferroelectric capacitors which hold their memory state in distortions of their crystal lattice with or without a circuit attached. An autonomous memory circuit utilizes this property to operate without clocks or control lines. A nonvolatile latch that is truly autonomous can operate with as few as three connections: ground, power, and the output node as shown in Figure 1. The output node provides the internal state of the latch to the outside world while the latch is powered up. It also acts as the input. The state of the latch is changed by forcing the output node of the latch to the desired digital condition. The latch then holds that new state as long as power is applied and returns automatically to that state when power is removed and reapplied. Thus, the nonvolatile latch operates autonomously and may be used in any electrical circuit with or without controlling logic or logic level voltage supplies. Other configurations of the autonomous latch can use separate input and output lines or an output line with two input lines, one for each state.

Figure 2 displays a function diagram for an autonomous nonvolatile latch built around a ferroelectric capacitor. While powered up, that latch will hold its state. The Data Switch is held ON or OFF by the Feedback Switch. The Feedback Switch is, in turn, controlled by the Input/Output node which reflects the state of the Data Switch. During power up, the ferroelectric capacitor/sense capacitor pair is energized passively by Power through the Conductive Load. The voltage on the Sense Capacitor determines whether the Data Switch turns on or remains off. The detection threshold of the Feedback Switch delays its operation until after the Data Switch has made its selection, thereby locking in the state.

Figure 3 is one implementation of the autonomous nonvolatile latch of Figure 2 using bipolar components. The NPN transistor T1 is the Data Switch while the PNP transistor is the Feedback Switch. The diode drop of the PNP base circuit provides the detection threshold necessary for the Feedback Switch to delay its activation. During power-up, the voltage at Node A must lag behind the Power voltage to turn on the Feedback Switch. If no lag develops, the Feedback Switch remains off, the Data Switch remains off, and the output Node A is high. If a lag develops at Node A, the voltage on the control input of the Feedback Switch meets the conditions necessary to turn it on which then turns on the Data Switch. Node A is pulled low and remains low as long as the circuit is powered or until an external circuit pulls Node A high to set the opposite state.

The voltage at Node A is affected by the conduction state of the Data Switch which in turn is affected by the voltage on the sense capacitor. The area of the ferroelectric capacitor, the resistor values, and sense capacitor value are selected to match the expected rise time of Power so that the voltage at Node A lags behind Power if the ferroelectric capacitor starts in the DOWN state and begins to switch UP but not if the ferroelectric capacitor starts in the UP state and does not switch. The Conductive Load may be of any type, including a transistor or a relay coil, while the sense capacitor can be a traditional linear capacitor, a ferroelectric capacitor, a resistor, or another charge-to-voltage or current-to-voltage generator. The Feedback Switch and Data Switch may be selected from a variety of technologies including FETs, MEMs relays, and ferroelectric gate transistors used as logic switches.

The author constructed the circuit of Figure 3 using integrated ferroelectric gate transistors [6] packaged in TO-18 transistor packages. Typical integrated ferroelectric gate transistors are shown in the die photo of

Figure 8. The data capacitor and sense capacitor, bonded from the die in photo in Figure 7, were packaged together in a single TO-18 transistor package. The ferroelectric capacitors consisted of 1200Å 20/80 PZT with platinum electrodes. The data capacitor had an area of 1,000 μ^2 while the sense capacitor had an area of 10,000 μ^2. External components were connected to the packages to complete the latch. A 220 pF linear capacitor and a 50 MΩ resistor were placed in parallel to the sense capacitor. A 1 kΩ resistor was used as the Conductive Load. The circuit was driven and measured synchronously using a Radiant Technologies, Inc. Precision Premier II tester. Figure 4 shows the Output node of the circuit during power-up from the two different states. This plot looks very similar to that of a bit line in a FeRAM memory array with the exception that the states go in opposite directions for the FeRAM read operation than the autonomous memory latch operation. In the FeRAM, the signal of a ferroelectric capacitor in the DOWN state - pointing towards the plate line - goes to the supply voltage after latching. In the autonomous nonvolatile latch circuit, the DOWN state returns to ground. The advantage of using ferroelectric gate transistors with the ferroelectric capacitors is that the circuit may be fabricated on a single die.

A unique quality of the autonomous nonvolatile latch circuit is that it can be written when powered off. If the data capacitor is left in the UP state, after power down a voltage pulse of sufficient energy and potential applied to Node B of the latch will turn on the Data Switch and allow the ferroelectric data capacitor to switch to the DOWN state. See Figure 5. The write pulse may originate from another powered circuit or may be generated directly by a sensor monitoring an environmental condition. The latch may be turned on at a later time by applying a voltage to Power to determine if a sensor event occurred while the latch was powered off.

Another advantage of the autonomous nonvolatile latch is that it may operate without the presence of control logic, a microprocessor, or logic-level voltage supplies. For instance, with suitable passive voltage-step-down components added to the conductive load as in Figure 6, the latch may be powered from a higher potential voltage source. In the figure, the Rv resistors and transistor T3 establish a source follower circuit that steps down the system voltage to one that can be handled by the ferroelectric capacitor. The latch output controls the base of an open-collector NPN power transistor which in turn can control an industrial relay, the power state of an electric motor, or other industrial devices. A separate circuit or a pair of manual switches (not shown) is added to the latch output to set the state of the latch while it is powered on. In this circuit, the ferroelectric capacitor is not confined to the 5V range and may be deposited much thicker to operate more reliably at higher voltages. Eliminating the need for a separate conditioned power supply to energize traditional digital memory and its supporting circuitry significantly reduces system cost.

A memory that operates without a microprocessor or controller or clock eliminates complexity and enables new architectures unlike any that have been conceived before. Please contact Radiant Technologies, Inc.

References:

[1] J T Evans and R Womack, "An experimental 512-bit nonvolatile memory with ferroelectric storage cell", *IEEE J. of Solid State Circuits*, v23 No 5, pp. 1171-1175, Oct 88
[2] K Udayakumar et al, "Manufacturable High-Density 8Mbit One Transistor-One Capacitor Embedded Ferroelectric Random Access Memory", *Jpn J Applied Physics*, v47, pp. 2710-2713, 2008
[3] Y Shimojo et al, "High-density and high-speed 128Mb chain FeRAM™ with SDRAM-compatibleDDR2 interface", *2009 Symposium on VLSI Technology*, pp. 218-219, June 2009
[4] K Dimmler and S Eaton, "Memory cell with volatile and non-volatile portions having ferroelectric capacitors", *US Patent 4809225*, February 28, 1989
[5] J Eliason, "Ferroelectric Nonvolatile Logic", *Integrated Ferroelectrics*, v40 n1-5, pp. 3-14, 2001
[6] J Evans and J Bullington, "Ferroelectric non-volatile variable resistive element", *US Patent 5070385*, December 3, 1991

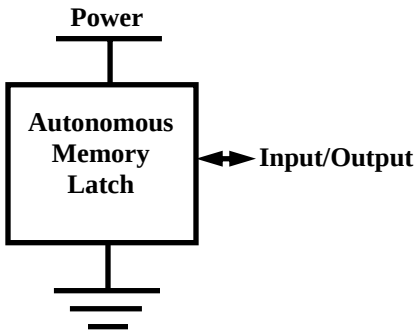

Figure 1: Symbolic diagram of simple 3-line autonomous memory latch. The device has no control lines or clock and the output is also the input. An external circuit may force its output high or low. Once set, the state remains even through power cycles.

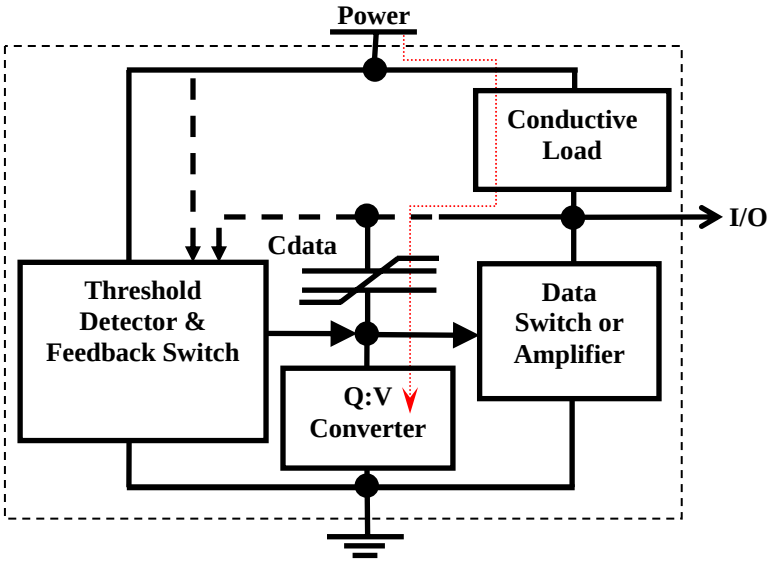

Figure 2: Functional implementation of autonomous memory latch. The red dotted line indicates current flow to the ferroelectric capacitor and sense capacitor during power up. Power up also is the read operation. The comparator/switch reinforces the state generated by Cdata during power-up.

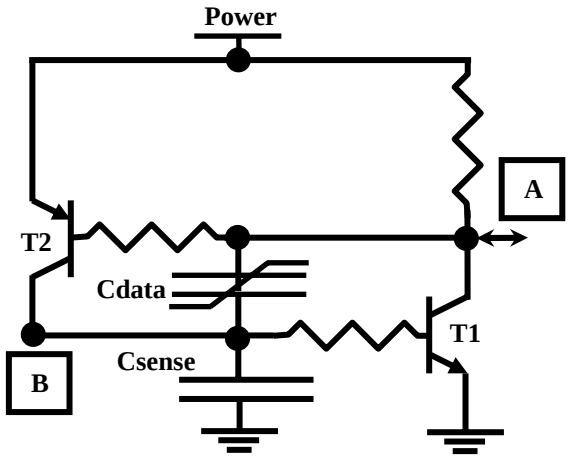

Figure 3: **Circuit diagram for bipolar implementation of an autonomous nonvolatile memory latch. Node A is the combined output/input. Node B may also act as an input. The circuit will function with a variety of transistor or switch technologies.**

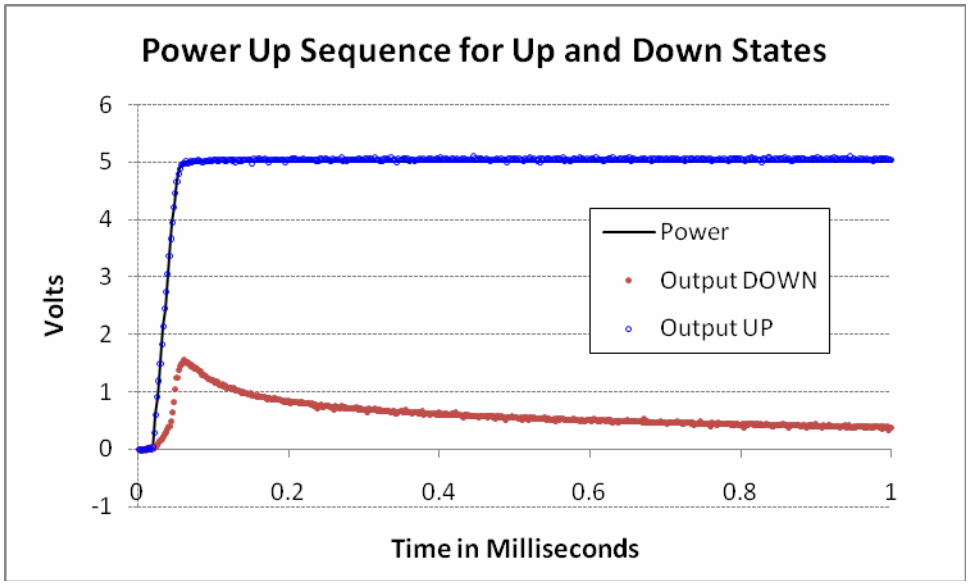

Figure 4: **Plot of the supply and output voltages during power up from the opposing retained states. The plot resembles the bit line operation of an FeRAM but the traces move in opposite directions from their counterpart states in the FeRAM.**

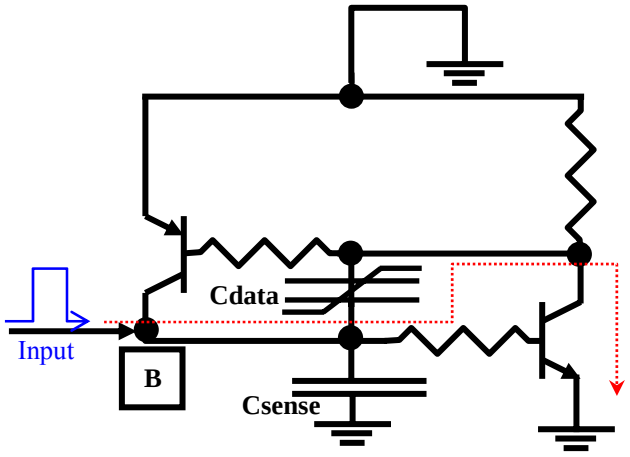

Figure 5: Write operation of the DOWN state into the ferroelectric capacitor in the autonomous nonvolatile latch while power is off.

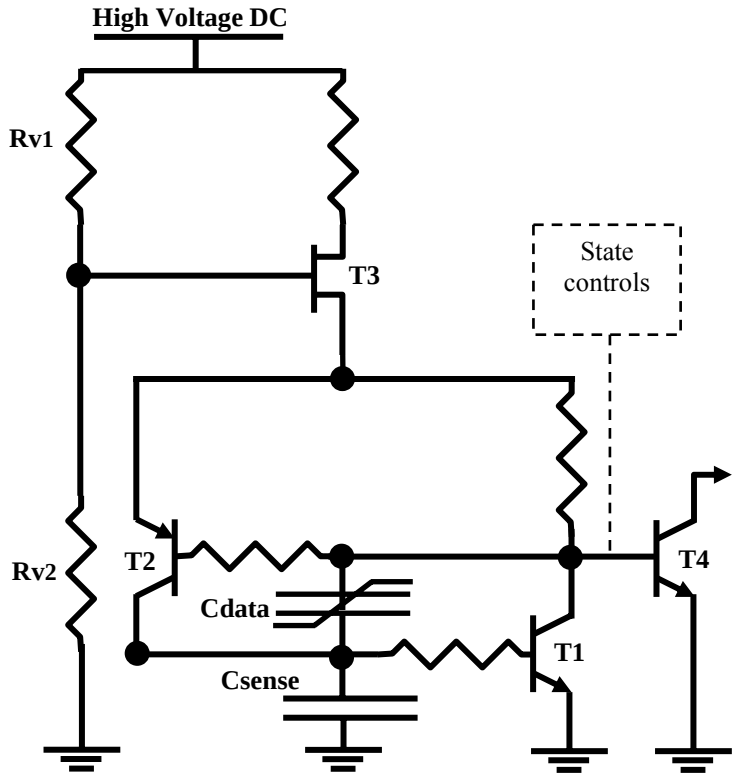

Figure 6: Autonomous nonvolatile latch operating from a high voltage supply controlling an external device through an open-collector NPN power transistor.

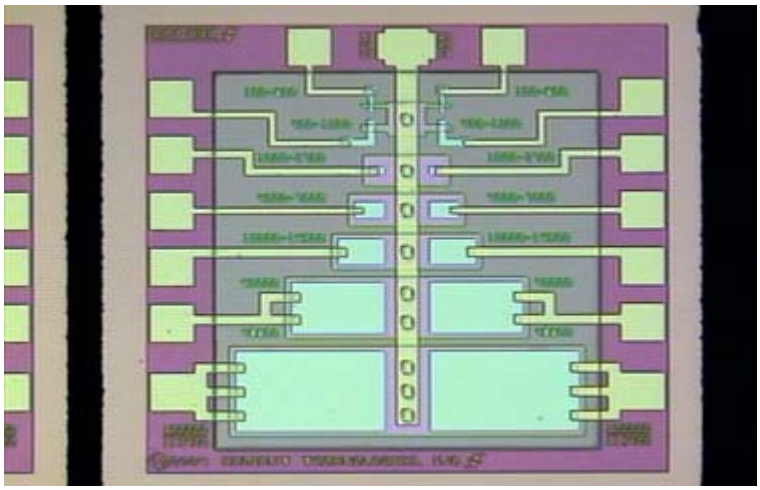

Figure 7: **Die photo of integrated ferroelectric capacitors used in the verification circuit.**

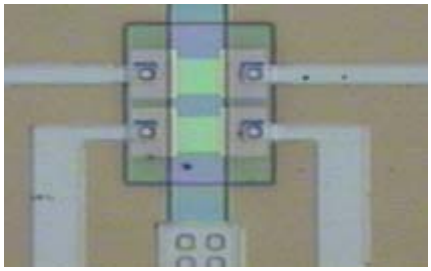

Figure 8: **Die photo of integrated ferroelectric gate transistors of the type used in the verification circuit.**