piezoMEMS Capacitor Degradation over Time & Temperature

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International Workshop on Piezoelectric Materials and Applications

Kobe, Japan

September 14, 2018

Summary

- Why test device *properties* instead of device *failure* over time?
- Experiment samples, fixture, and procedures
- Results
- Conclusions

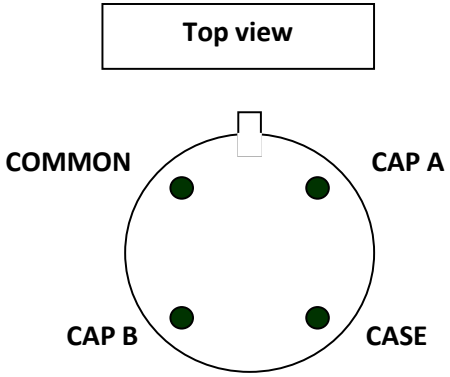
Why Test Properties?

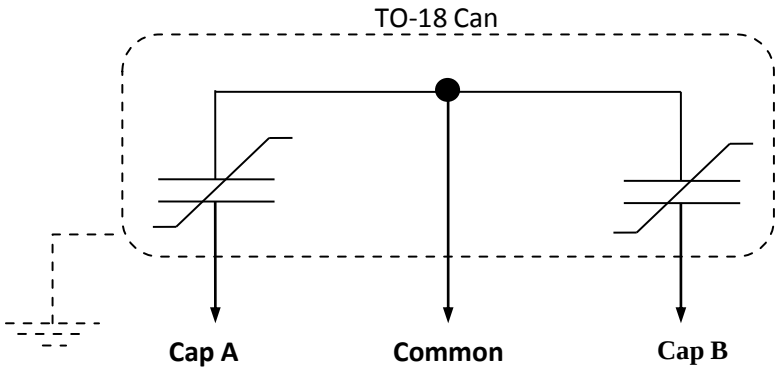
- Many non-linear devices depend upon *inherent memory* for their function: *This includes any piezoelectric device that requires poling.*
- Memories accumulated by such a device over its lifetime cause its performance to change. This is traditionally called "ageing" but it actually affects all properties.
- pMEMS devices might not suffer catastrophic failure but instead the drift in their properties over time *can lead to system failure*.

Testing Property Drift

- The authors characterized drift in device properties for packaged thin-PZT-film capacitors using automated testing techniques.
- The capacitors were 250nm-thick, 2% niobium-doped 20/80 PZT with platinum electrodes. (PNZT)
- Hundreds of measurements were required to produce compact representation of property drift.
- The following pages describe the fixturing and automated test procedures used to characterize the properties of the PZT capacitors.

Sample Preparation

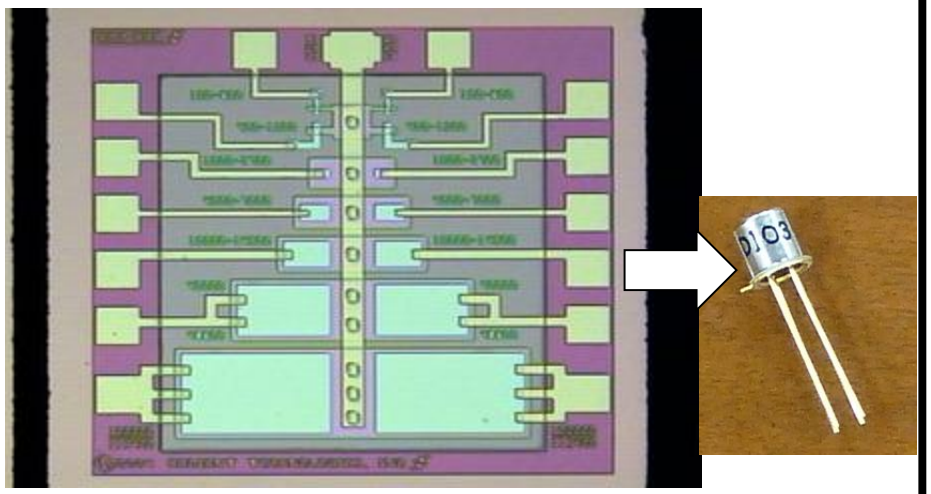




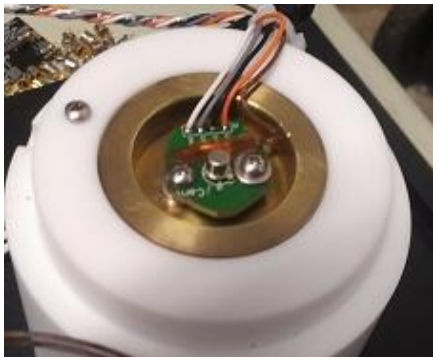
Capacitor dice were packaged in TO-18 transistor packages using Cr/Au bond pads and gold bond wires.

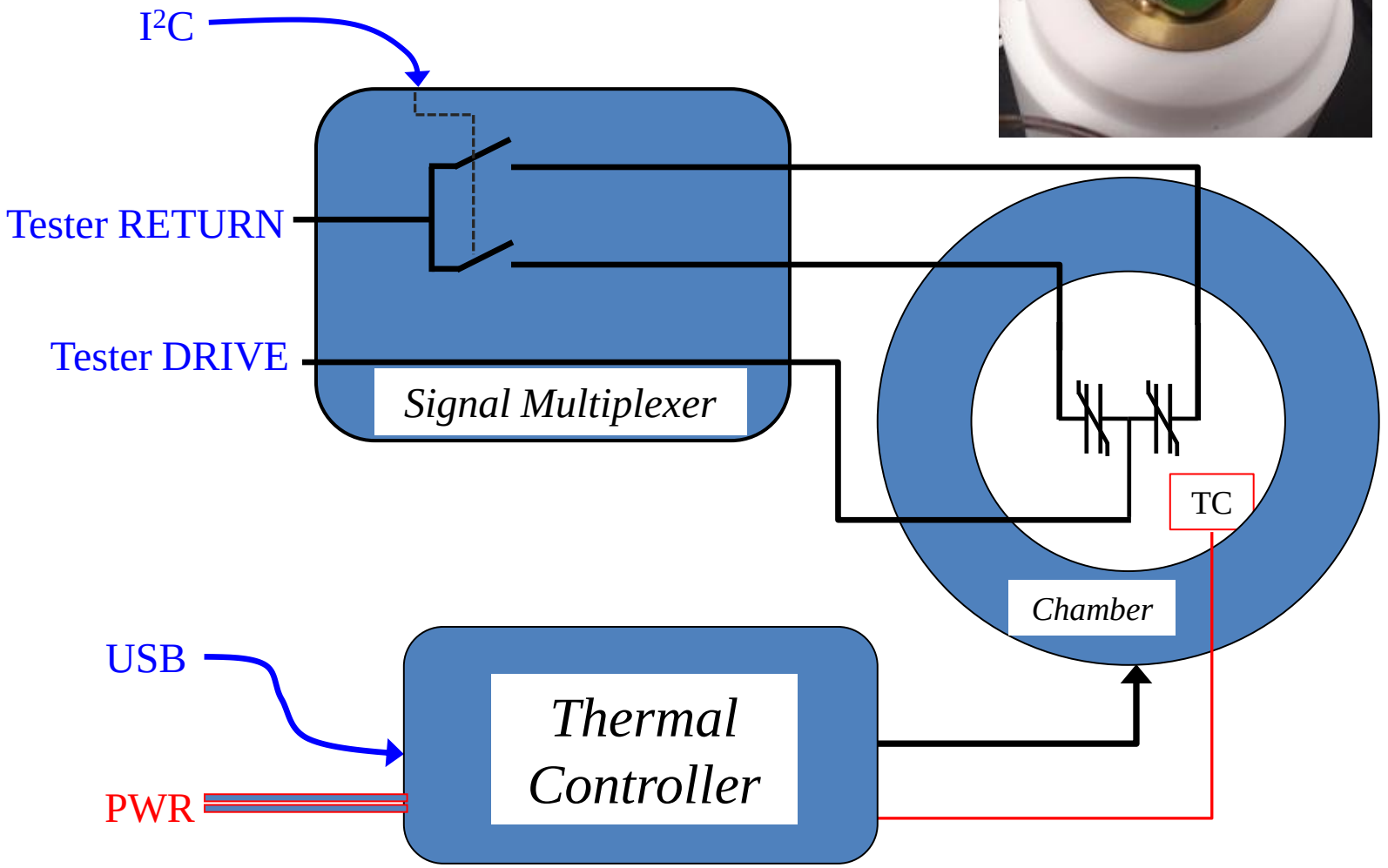
Lids were not sealed hermetically.

The packages were inserted into a thermal chamber for test.

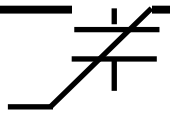


Test Fixture



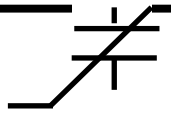


Test Procedures



→COMBO Test	A series of *Wake-up* stress tests applied at room temperature immediately after fabrication.
→Temperature Cycle	Measure changes in properties during two *Temperature Cycles* from room temperature to 90C.
→Retention/Imprint	Measure changes in *Retained State* and *Opposite State* polarizations with time at temperature.

Test Procedures



→Fatigue

Measure polarization loss due to *Voltage Cycling* at temperature.

- Switched polarization for memory.
- Monopolar cycling for actuators.

→HALT

Measure change in capacitor properties with *Time-At-Temperature* under *DC Electrical Bias*.

- Typically executed at 300kV/cm for thin films.

Conducted in this order using 3 packages of two capacitors each requires 6 days.

COMBO Test Definition

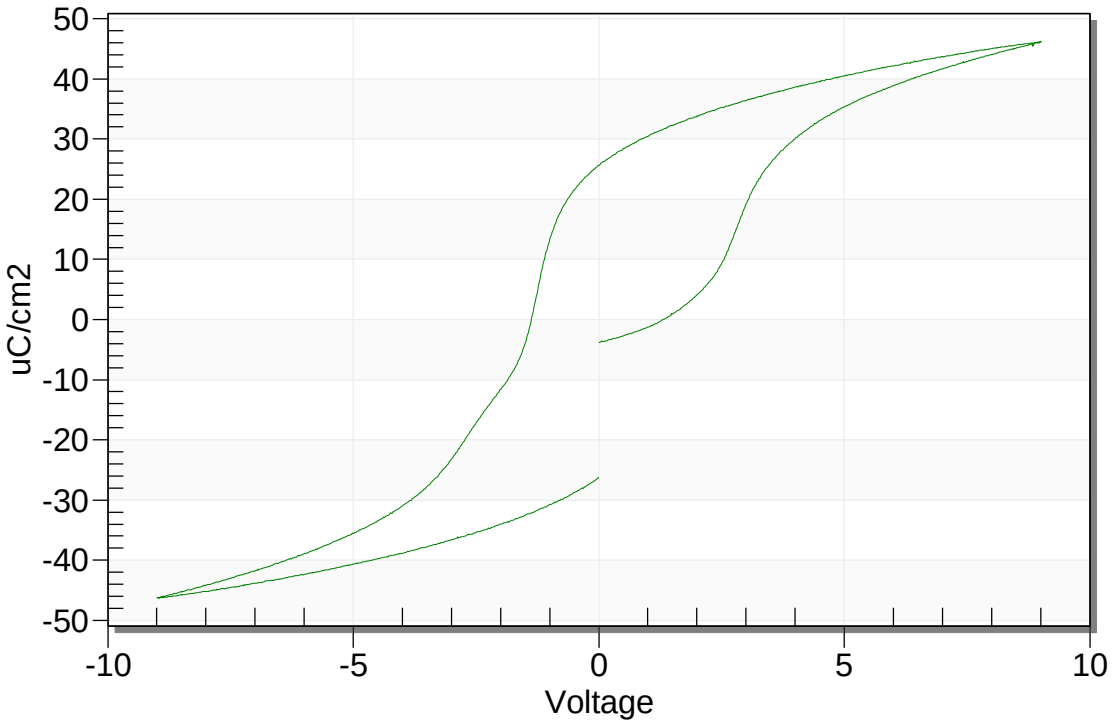
The COMBO test subjects the *virgin sample* to multiple cycles to evaluate film quality.

1. Subject a capacitor to multiple wake-up cycles of square waves and sine waves.

2. Measure hysteresis after each cycling period.

COMBO Test Result

Virgin Loop

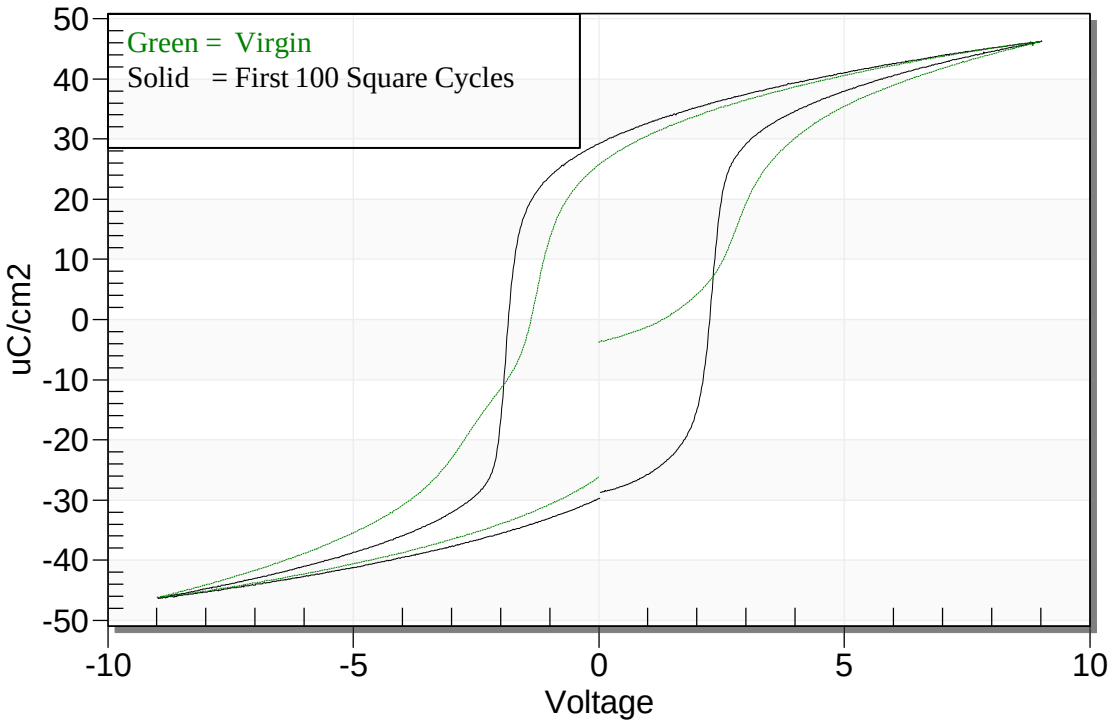


The very first *virgin loop* after fabrication. It started exactly at *zero polarization* as expected indicating random domain orientation as-made.

Total = 1 Hysteresis Cycle

COMBO Test Result

100 Cycles 1Hz Square Wave

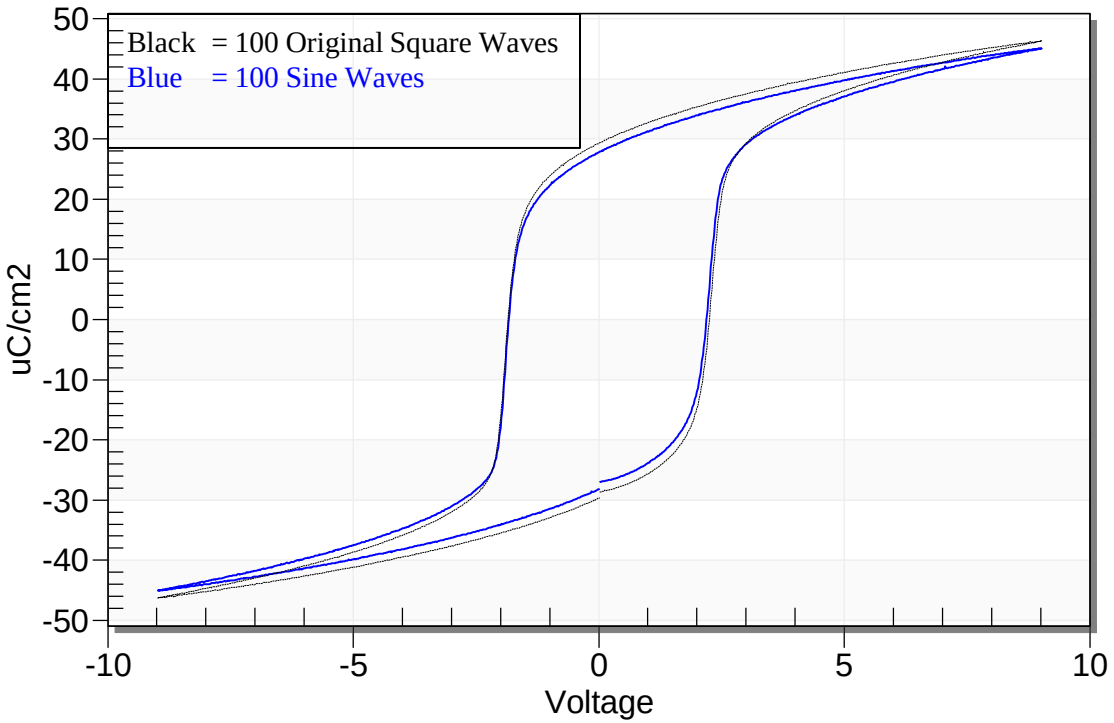


These 100 cycles are called *Recovery* at Radiant. The device shows improved hysteresis loop after Recovery.

Total = 101 Hysteresis Cycles

COMBO Test Result

100 Cycles 1Hz Sine Wave

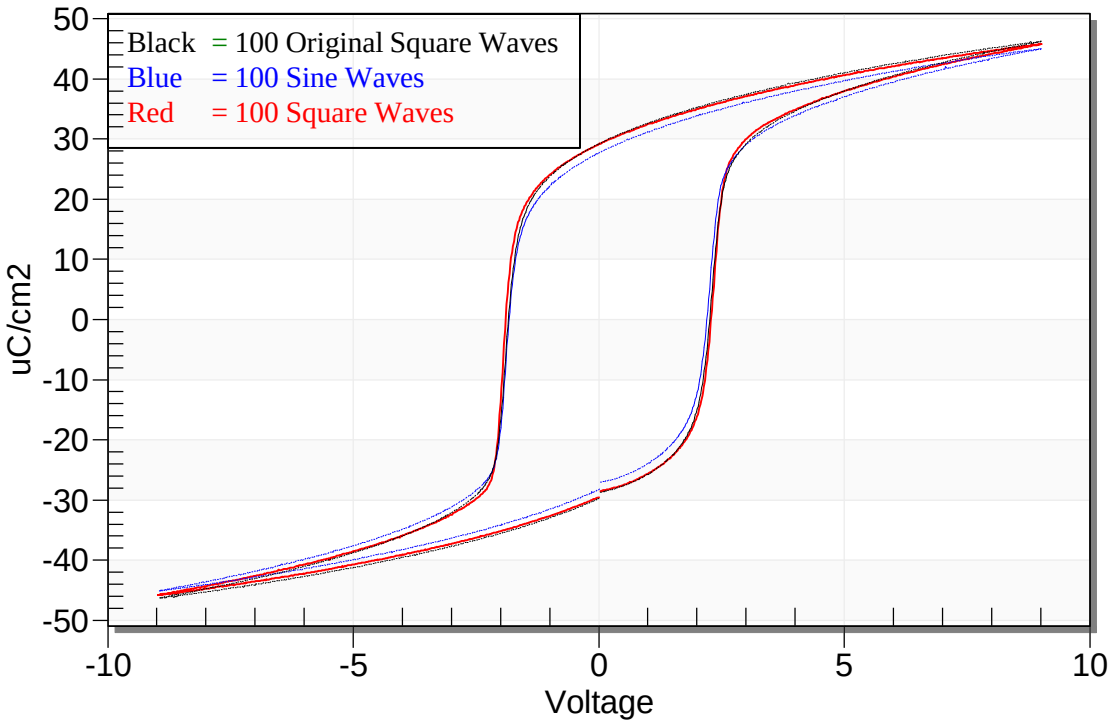


The next 100 cycles were *Sine Waves*. Sine waves always cause Pmax to *decrease*. The reason is not known but the amount is affected by process.

Total = 203 Hysteresis Cycles

COMBO Test Result

100 Cycles 1Hz Square Wave



The next 100 cycles are *Square Wave*. *Pmax was restored* to near its original value. This performance meets the process target.

Total = 306 Hysteresis Cycles

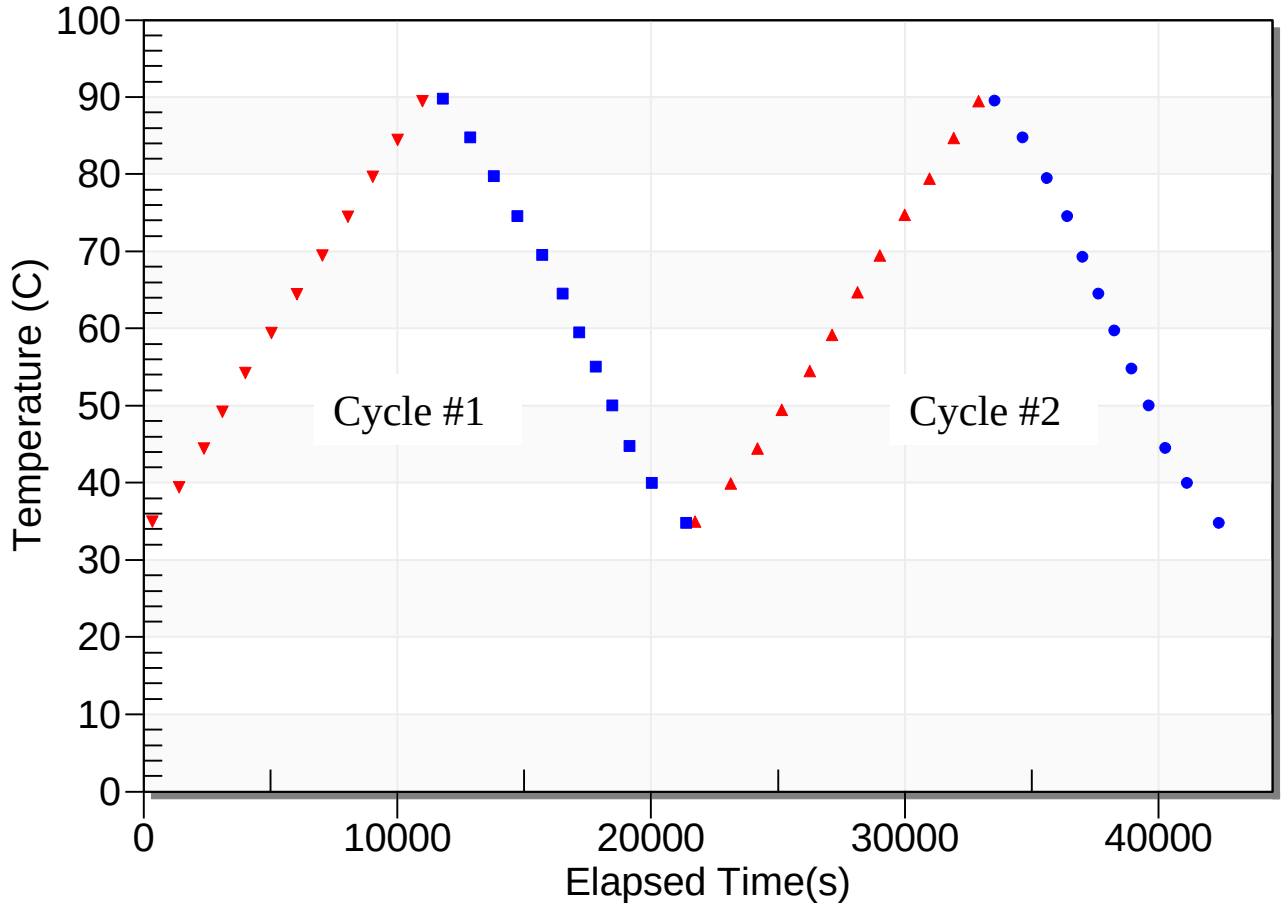
Temperature Cycles

Measure capacitor properties over temperature *after Recovery*.

1. Program two temperature cycles from room temperature to 90C and back in 5C steps.

2. Measure Hysteresis, PUND, Leakage, and Small Signal Capacitance *every 5C* step after stabilizing at temperature.

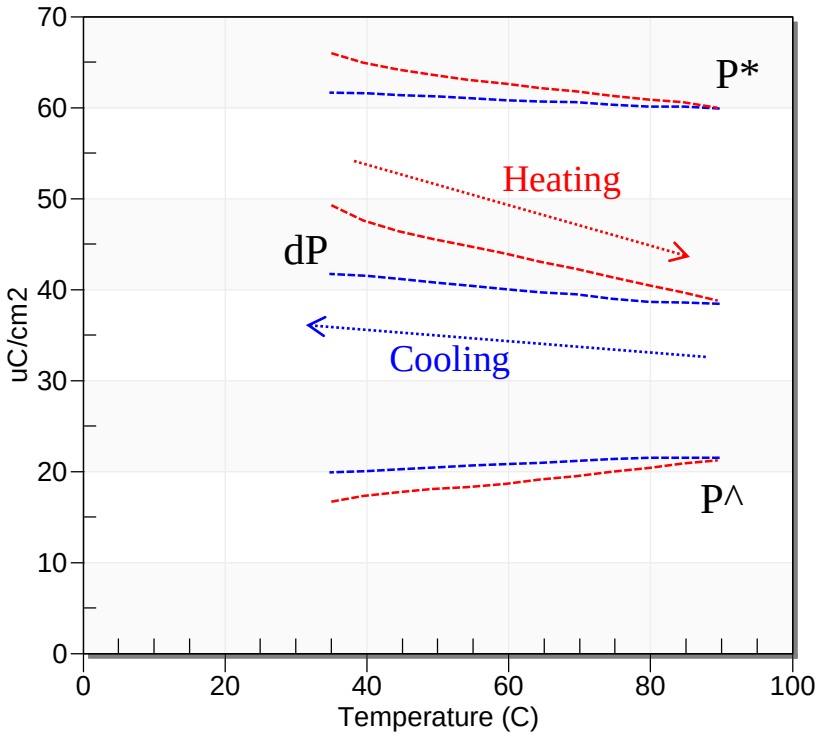
Temperature Profile



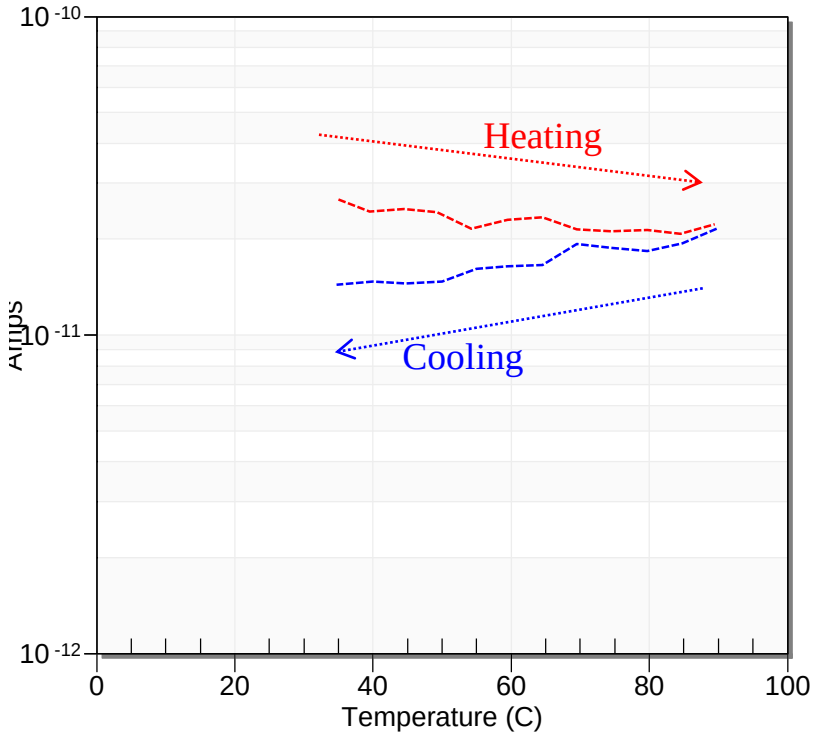
Temperature Cycles

Cycle #1

PUND P*, P^, dP



Leakage (A)



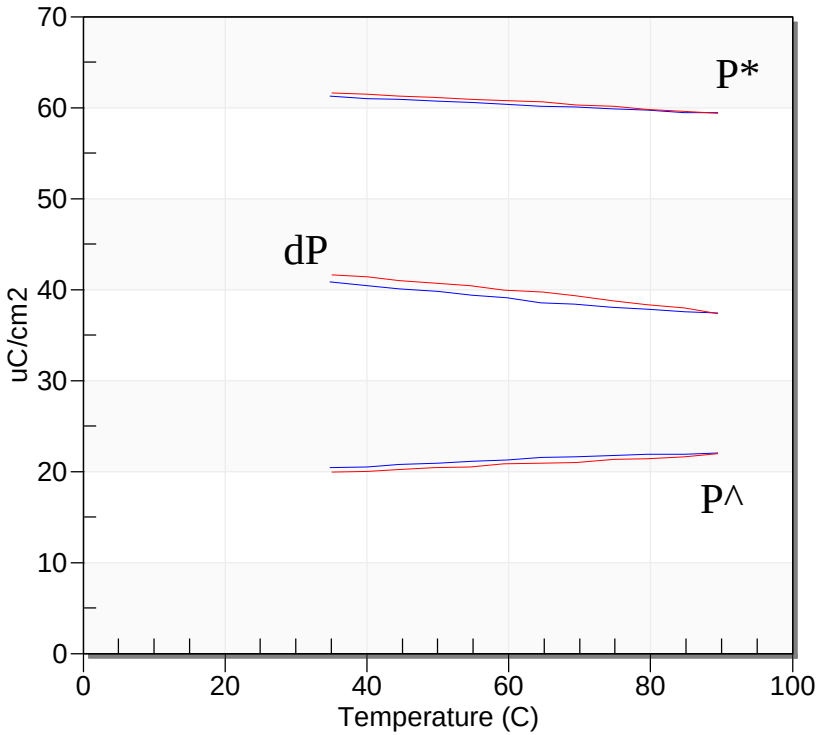
Both the PUND and the Leakage profiles on the first temperature cycle *aged quickly*. A degradation in polarization is observed.

Total = 144 Measurements over 24 Temperatures

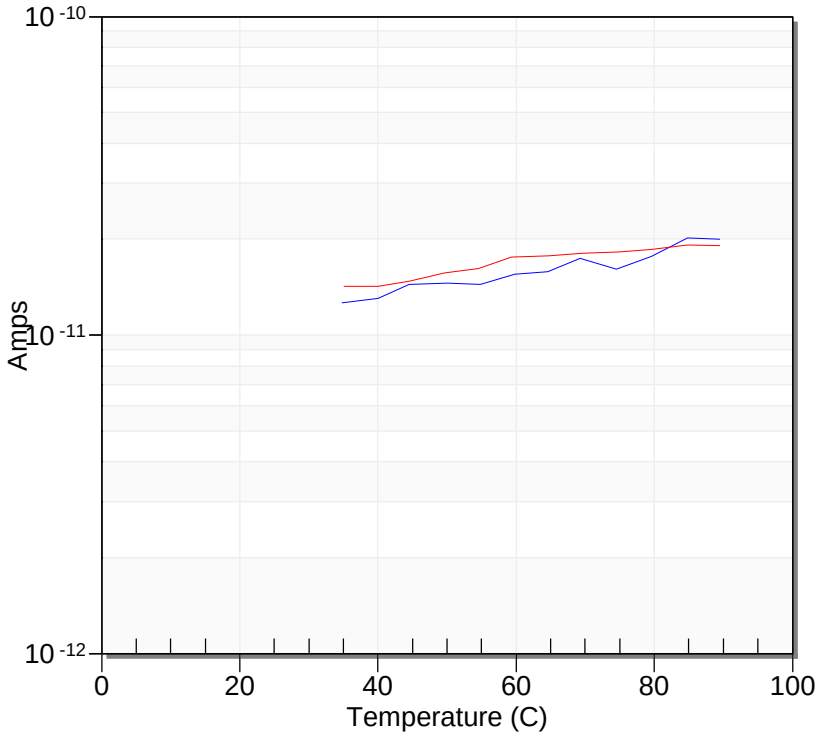
Temperature Cycles

Cycle #2

PUND P*, P^, dP



Leakage (A)



The changes in properties around the temperature loop stabilized during the second cycle.

Total = 288 Measurements over 48 Temperatures

Retention/Imprint

- *Retention* – Switched and unswitched polarization amplitudes retained *since last write event*.

- *Imprint* – 1-second Retention Test of the *opposite state* measured *immediately after the retention measurement*.

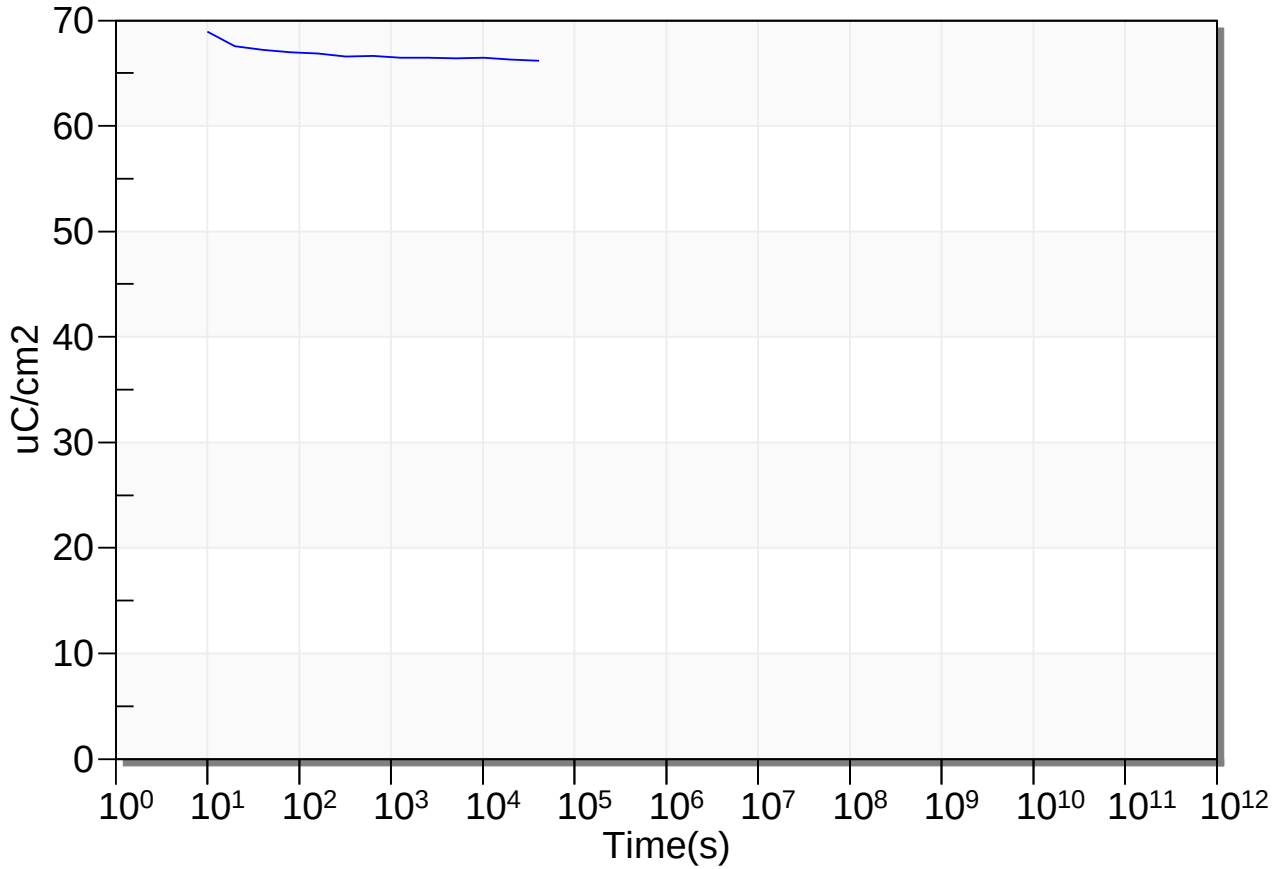
  1. Write Retained State.
  2. Retention Delay
  3. Read Retained State.
  4. Execute 1-second Retention Test of the *Opposite State*

Why Retention/Imprint?

- Retention and Imprint would seem to be important only to memory applications like FRAM.
- All piezoelectric properties of ferroelectric materials *arise from the remanent polarization*.
- Drift in unswitched Remanent Polarization will couple to *piezoelectric actuator performance*.

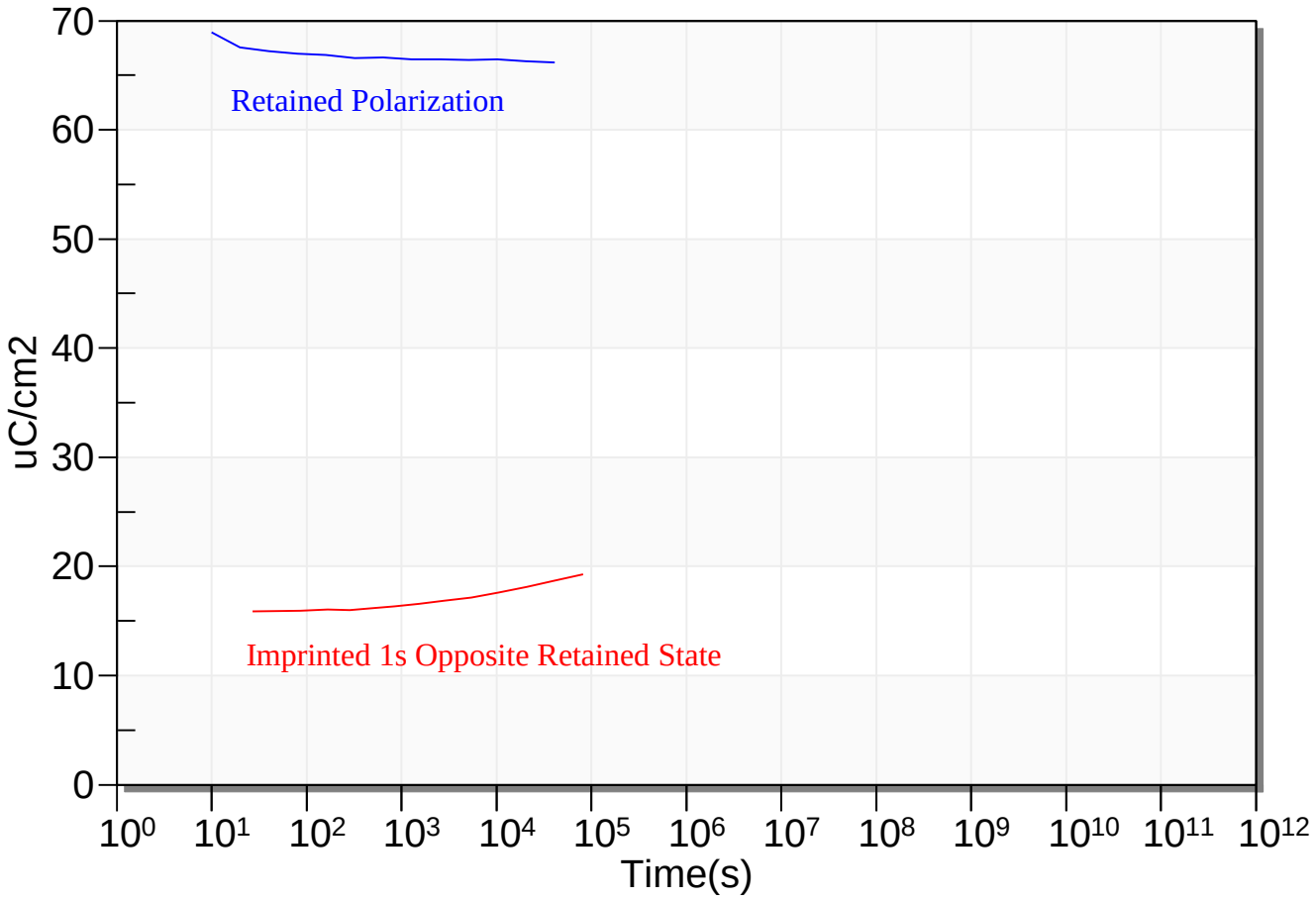
Switched Retention

Measured change in polarization over time



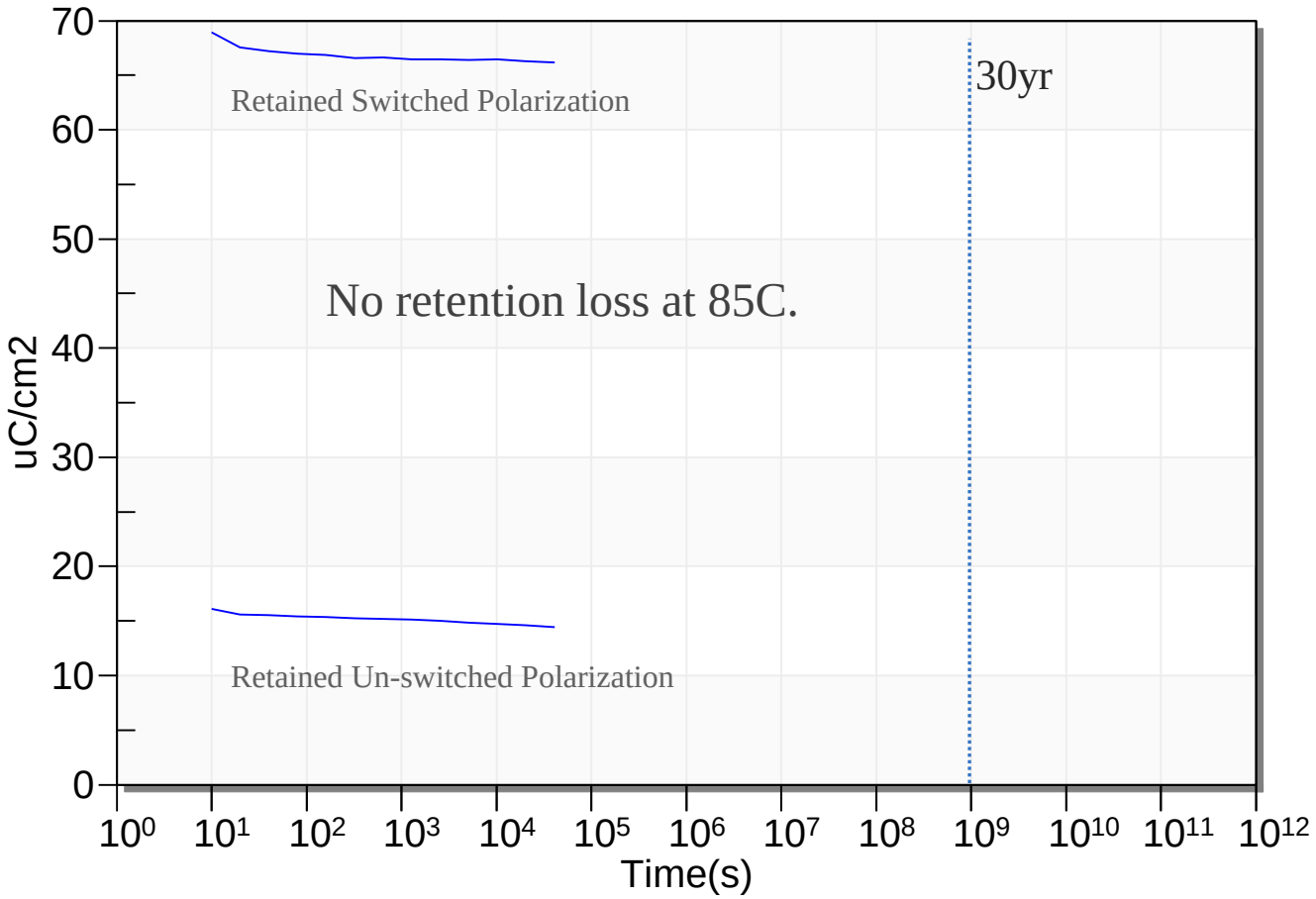
Total = 13 Measurements at 85C

Switched Retention/OS Imprint



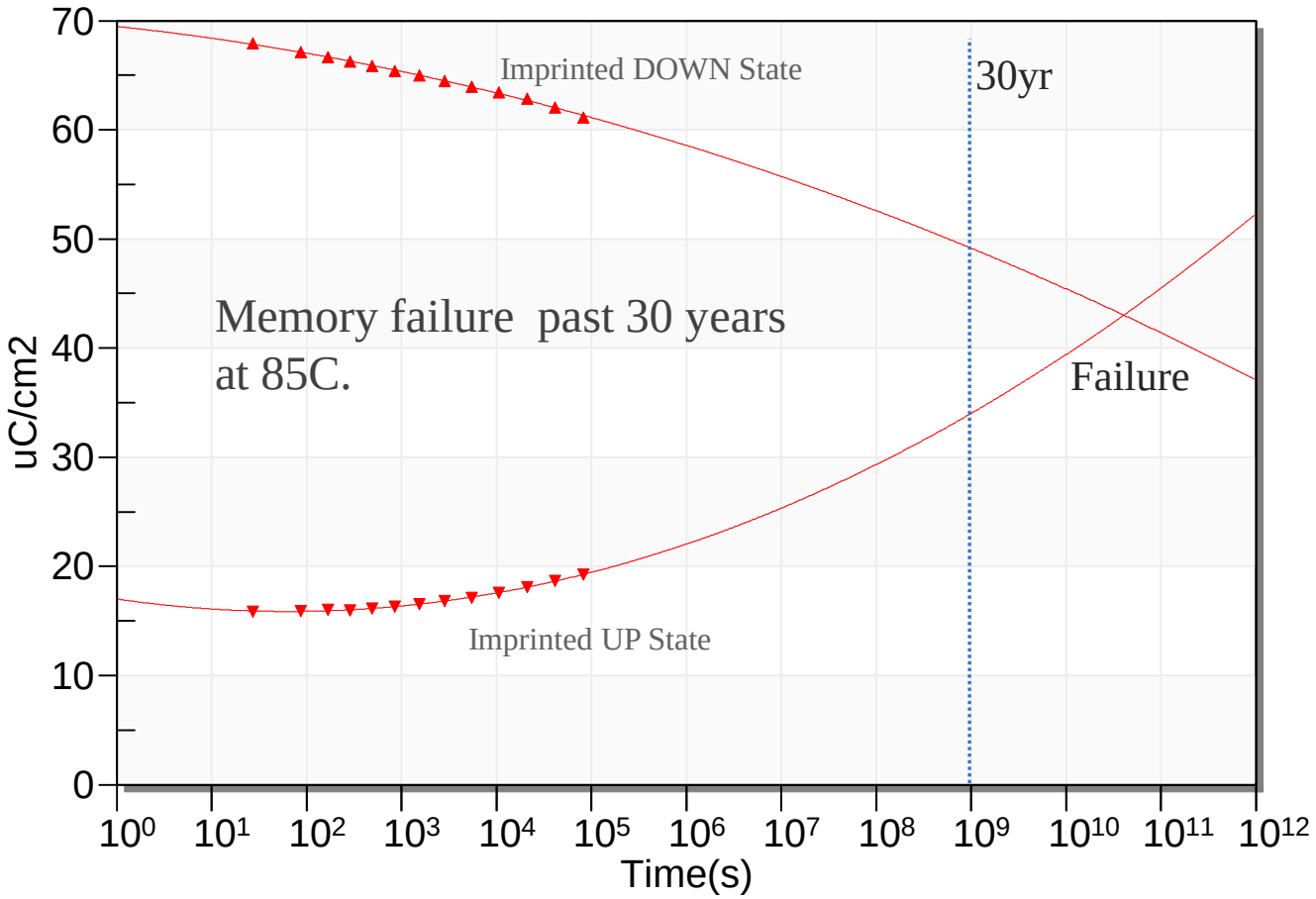
Total = 26 Measurements at 85C

UP/DOWN Retention



Total = 26 Measurements at 85C

UP/DOWN Imprint



Total = 26 Measurements at 85C

Bipolar Fatigue vs Temperature

Measure the change in capacitor property or properties as a function of polarization reversals.

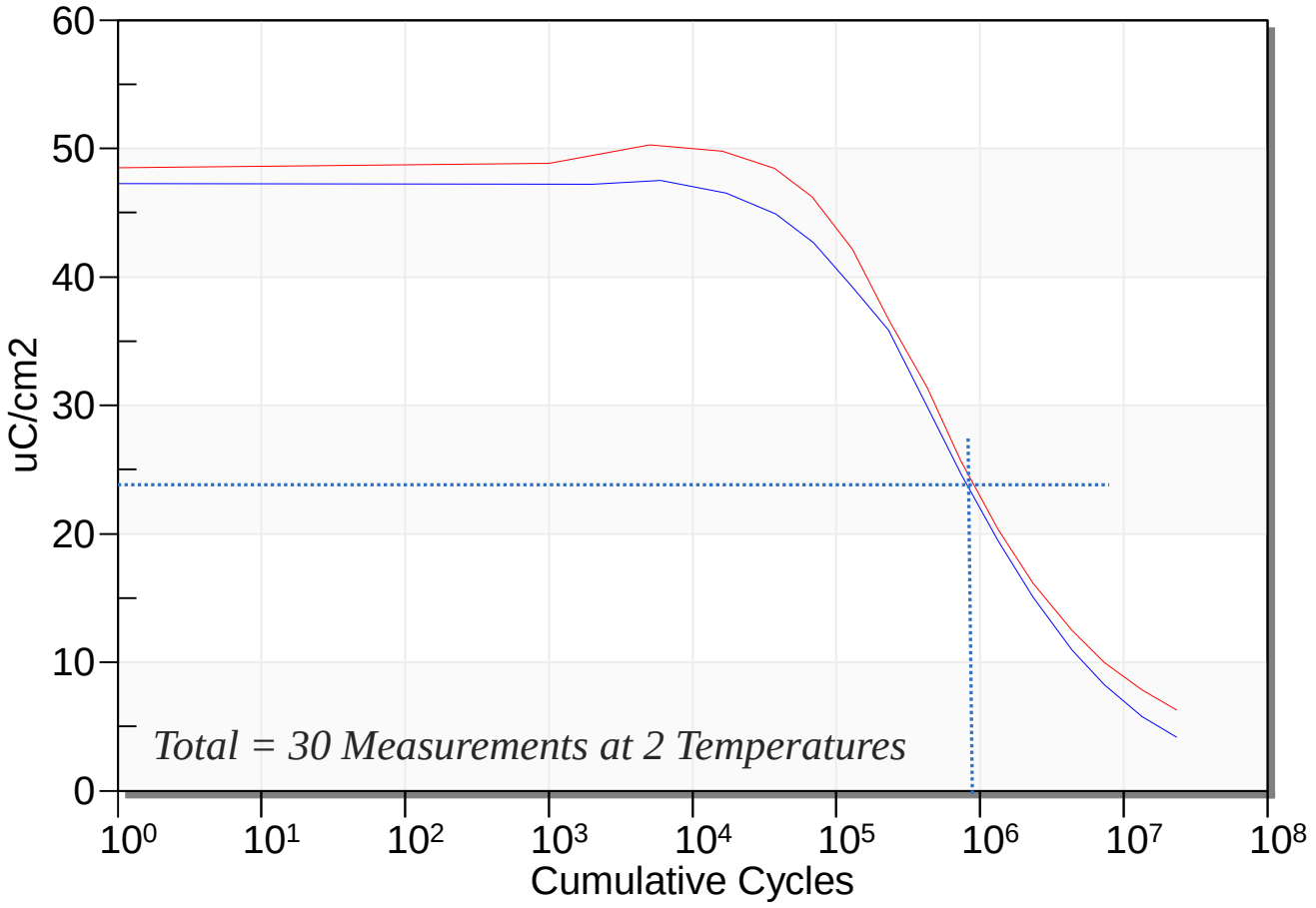
1. Execute 2 alternating ±7-volt cycles every millisecond for 1 second on an *imprinted* capacitor.

2. Measure *PUND* at 30C.

3. *Double the cycling time* and jump back to Step 1.

Repeat the same test on the second imprinted capacitor at *85C*

Bipolar Fatigue vs Temperature



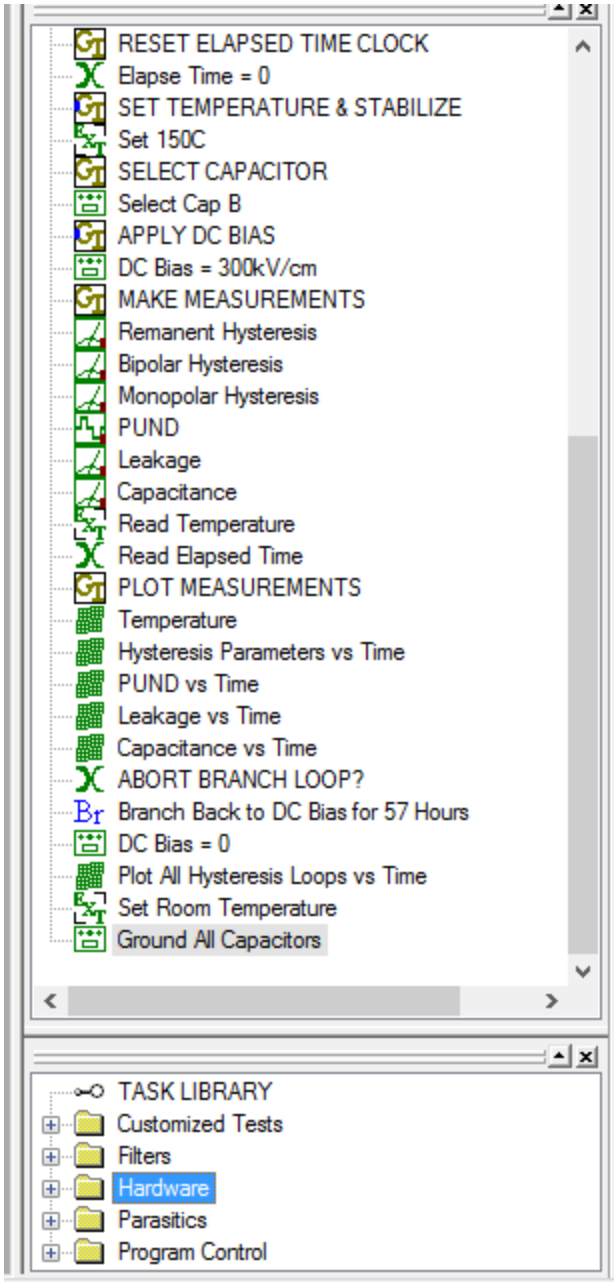
Fatigue was *unaffected by temperature*. Platinum-electroded capacitors reached 50% of starting Remanent Polarization at *1 million cycles*.

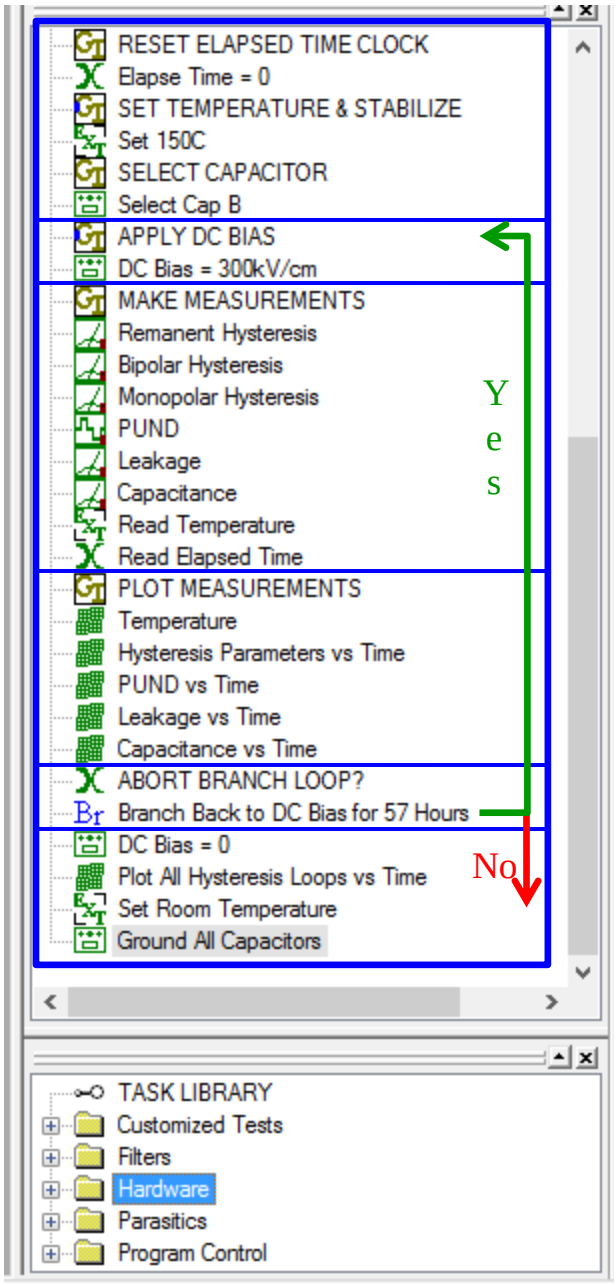
HALT

- HALT – High Accelerated Life Testing
  - Measure leakage growth over time with DC Bias at temperature
  - Typically the device is run to catastrophic failure.

- Non destructive HALT can also track properties over time.
  - All properties are measured over time under DC Bias at temperature
  - The test can be run to catastrophic failure but it is not necessary.

HALT Test Definition





HALT Test Definition

The Test Definition has 6 sections:

1. Set Temperature and Configure the Fixture.
2. Apply DC Bias for increasing time periods.
3. Measure All Properties
4. Plot All Measurements
5. Apply Branch Condition

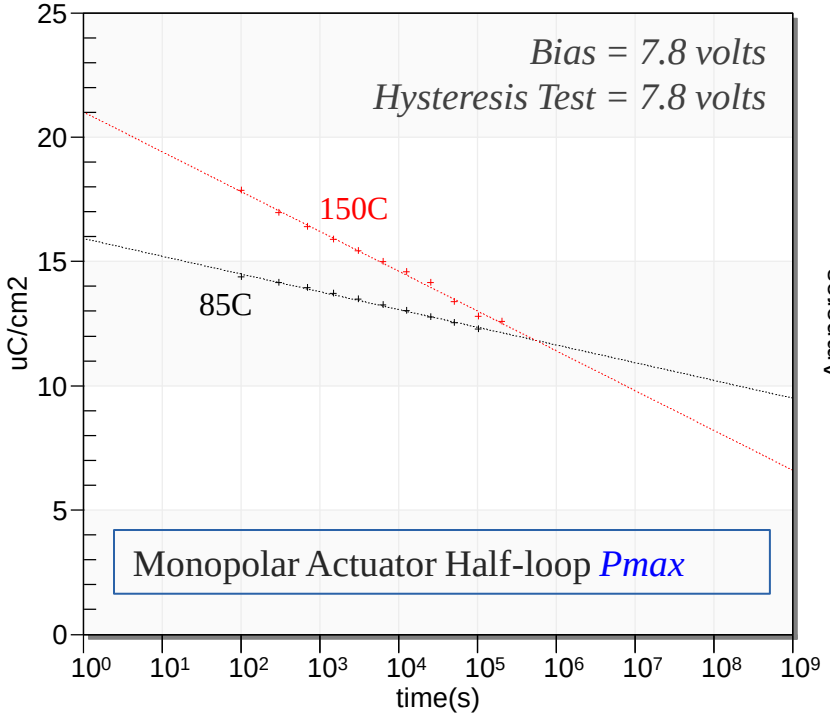
Yes

No

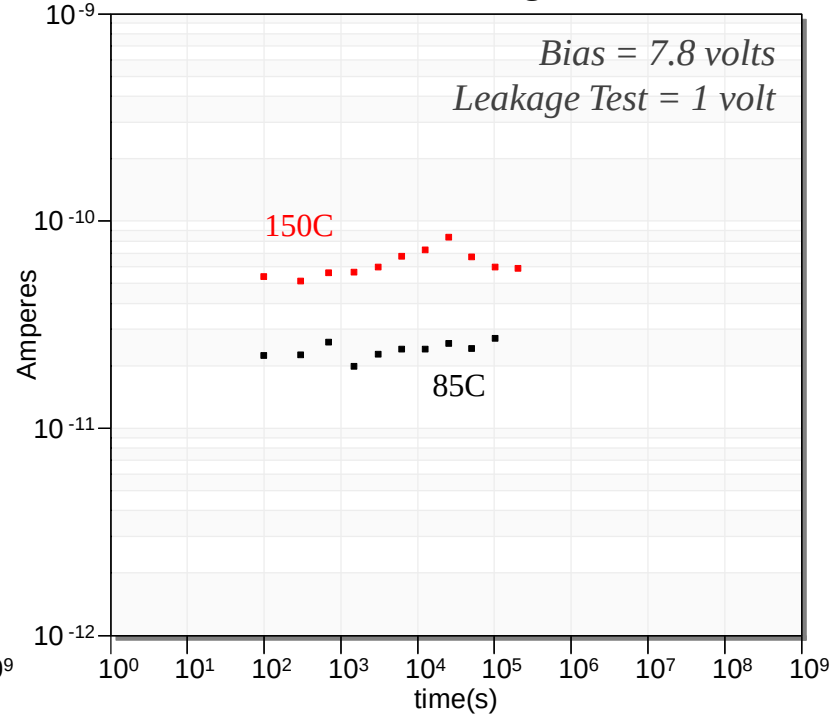
1. Shut Down and Exit

HALT @ 85C & 150C

HALT Hysteresis Parameters



HALT Leakage



The Hysteresis Pmax of a monopolar half-loop, as would be applied to a piezoelectric actuator, shows *DC Bias-induced Ageing* through the loss of Pmax with time.

Leakage remains below 1μA/cm^2 after 57 hours at 150C with *300kV/cm* DC Bias.

Total = 44 Measurements over 2 Temperatures

Conclusion

- 2/20/80 PNZT integrated thin-film capacitors were subjected to 420 measurements over a period of six days from 30C to 150C.
  - COMBO Test – Sample exhibited no Pmax decay indicating high quality film.
  - TEMPERATURE CYCLING – Rapid ageing caused initial polarization values to decay 15% during the first temperature cycle while leakage improved 46%. Properties were stable during second temperature cycle.
  - RETENTION/IMPRINT– Opposing capacitors tested simultaneously demonstrated unlimited retention at 85C with imprint failure beyond 30 years.
  - FATIGUE – Remanent Polarization decayed 50% at 10^6 reversals at both 30C & 85C .
  - HALT – Leakage change due to 300kV/cm DC Bias was minimal at both 85C and 150C over 57 hours. However, Actuator-type Pmax decayed 30% at 150C in 57 hours under the same test conditions.