

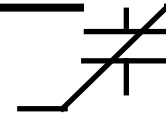
Architecture of the pMEMS Matrix Board and its Vision Tasks

Joe Evans

Radiant Technologies, Inc.

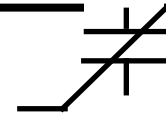
June 9, 2020

Summary



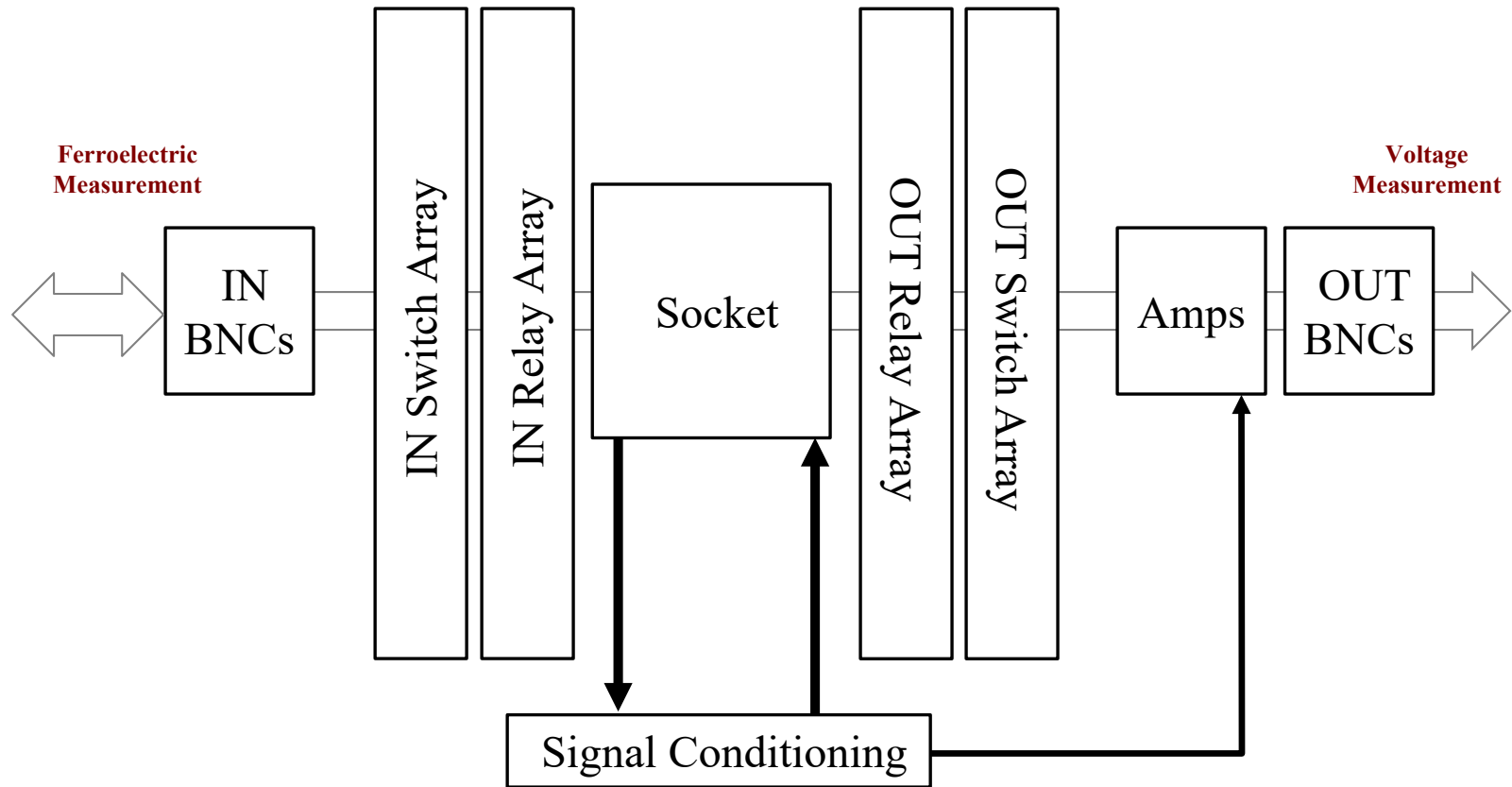
- The pMEMS Matrix Board is a platform to evaluate the operation, yield, uniformity and performance of piezoMEMS designs after fabrication.
- The Matrix Board will test DIP packages or connect to any fixture having BNC connectors such as probe stations, thermal chambers or signal multiplexers.
- Six external signals, connected to a bank of twelve relays, are routed dynamically by Vision to pins of the sample package during test execution.
- Two Tasks in the Vision Library allow the user to configure the Matrix Board for use.

Summary



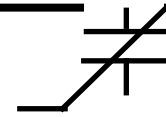
- The Matrix Board is divided into four sections:
 - 1) **IN:** BNC connectors, a switch array and six relays connect ferroelectric or piezoelectric capacitors on the pMEMS die to a Radiant pMEMS tester for characterization and poling.
 - 2) **OUT:** Six relays and a switch array connect outputs from the pMEMS die to amplifiers driving cables to the SENSOR analog voltage inputs and/or the Frequency Counter of Radiant's pMEMS tester.
 - 3) **FEEDBACK:** Two amplifier-driven paths with isolation relays will condition the sensed signal from a pMEMS pin for feedback to another pMEMS pin.
 - 4) **Support Circuitry:** An array of solder holes plus a connector to the parallel Digital I/O port or I²C port of the Radiant pMEMS tester supports installation of circuitry or a microprocessor that can independently operate the pMEMS under test.

Test Flow Diagram



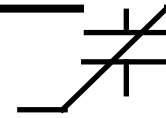
- The board divides in half logically. The left connects to ferromagnetic measurement channels. The right to voltage measurement channels.

Theory of Operation



- The Matrix Board signal flow is from *left-to-right*. (Except when not, as in when signals are passed to the tester RETURN channel?)
- On the **left side** of the board:
 1. **Three BNCs** (IN-A, IN-B and IN-C) accept signals expected to go directly **to** or **from** any pin on the sample package. For instance, DRIVE and RETURN connect here for Hysteresis measurements.
 2. **Manual DIP switches** connected to each BNC determine which IN signal connects to the input of which IN relay on the **SPi bus**. (Serial Peripheral Interface.)
 - a) Manual switches *cannot be changed* during execution of a Test definition.
 3. The operator selects **IN Relays** to be opened and closed *during* Test Definition execution to connect pins on the package under test to **IN BNC** signals through the **SPin bus** and **switch array**.
 - a) Relays can be turned on and off any number of times during a Test Definition using **the pMEMS Matrix Board Relays Task** from the Vision Library.

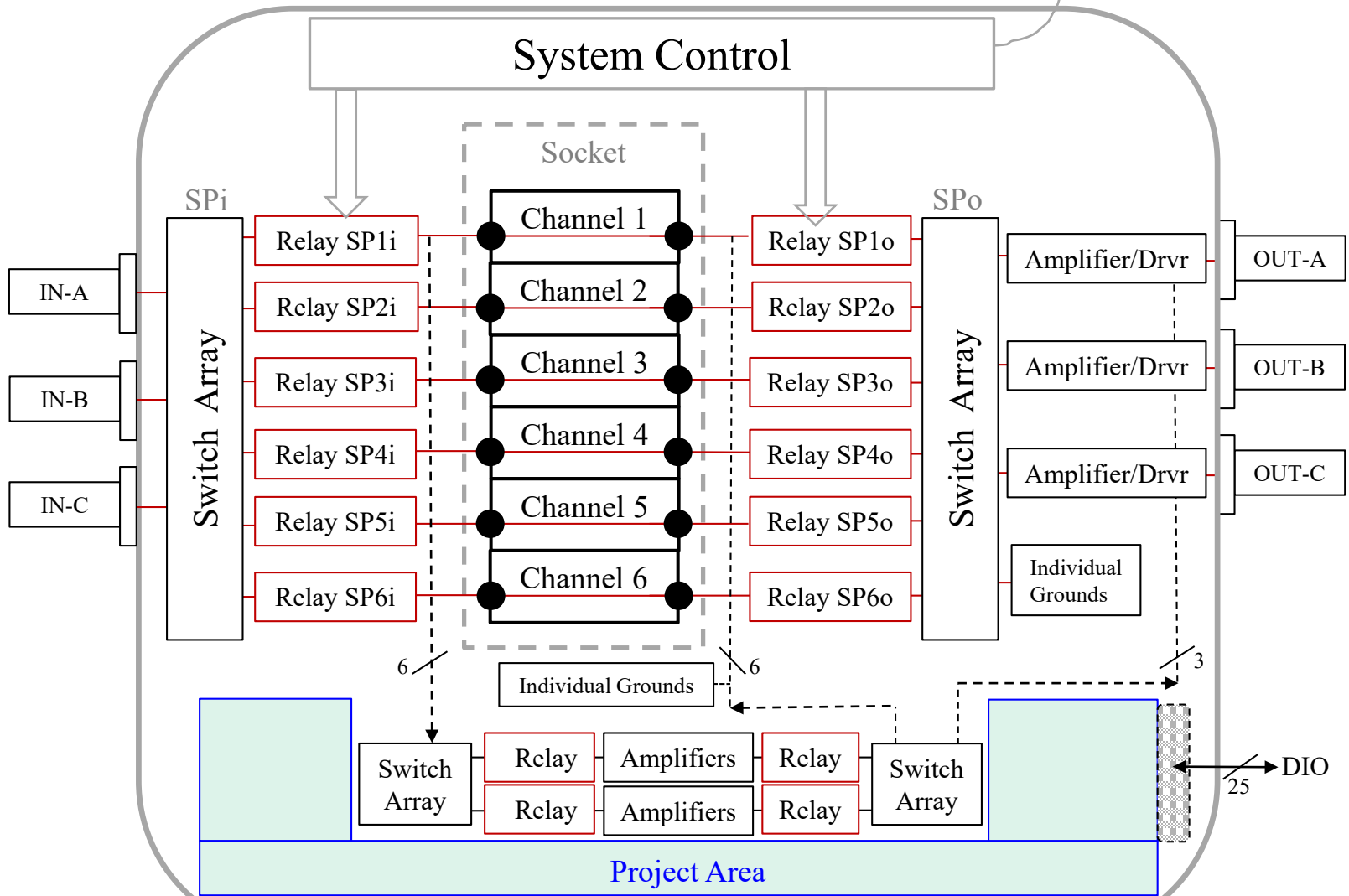
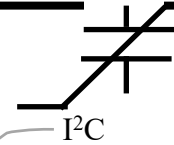
Theory of Operation



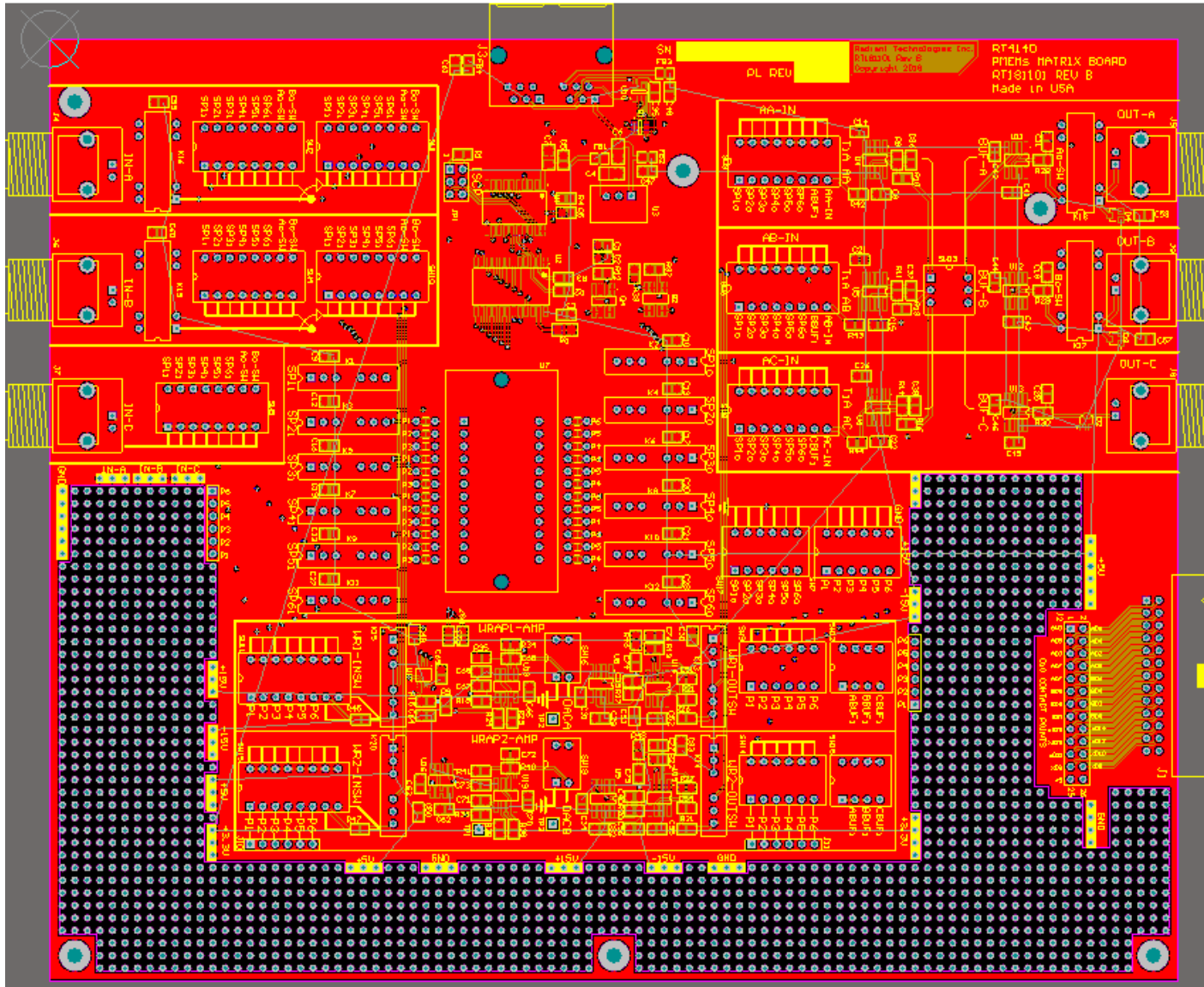
- On the **right** side of the board:
 1. Six **Out Relays** connect the pins of the sample to the **SPout** bus during Test Definition execution.
 2. Manual **DIP switches** connect the **SPout bus** to the inputs of the **OUT amplifiers** to send selected signals through the **OUT BNCs** (OUT-A, OUT-B and OUT-C) to external test equipment.
 - a) Manual switches cannot be changed during execution of a Test definition.

- At the **bottom** of the board sit the **Feedback Path Amplifiers**:
 1. Manual **DIP switches** connect the inputs of the **Feedback Input Relays** to selected pins of the sample under test. Only one input is allowed per feedback path.
 2. Manual **DIP switches** on the output of each **Feedback Output Relay** connect that relay to the **SPo bus** and/or **Cable Drivers**.
 3. The **Feedback Input** and **Output Relays** are controlled dynamically during Test Definition execution.

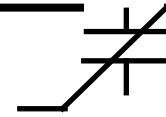
Detailed Floor Plan



Matrix Board PCB

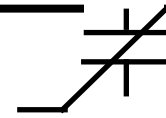


Notes



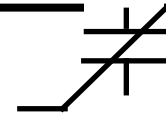
1. Sample packages are inserted into the Zero Insertion Force (ZIF) socket in the center of the board.
2. A daughter board accessory for the ZIF socket contains four (4) SMA connectors so probe stations, thermal chambers or multiplexers can be connected to the Matrix Board in place of a packaged sample.
3. The IN BNCs on the left-hand side of the floorplan connect directly to their cross-coupled switch block. **Signals may travel *in or out* of the IN BNCs.**
4. The OUT BNCs on the right-hand side of the floorplan are permanently driven by voltage follower op amps to drive BNC cables. **Signals may only travel *out* the OUT BNCs.** Each of the three cable drivers may take input directly from a feedback amplifier or from its own pre-amplifier connected to the SPout bus.
5. The outputs of the two feedback paths connect directly to pins on the die, ***not to the SPin and SPout buses*** on the inputs of the relay banks.

Notes



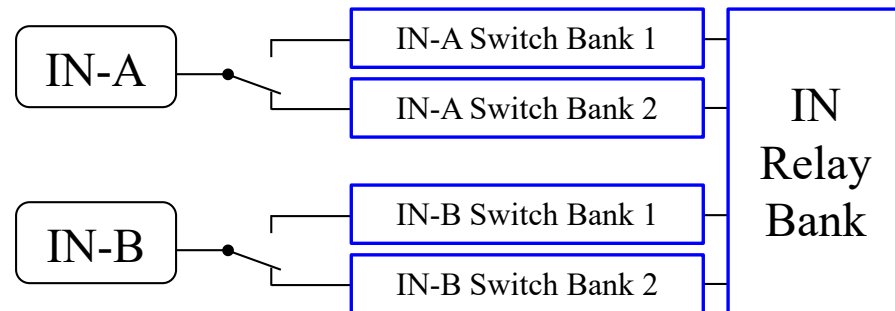
5. The feedback amplifiers and the OUT pre-amplifiers may be configured as voltage amplifiers or as transimpedance amplifiers by substituting 0805 surface mount resistors and capacitors.
6. The feedback amplifiers paths each host solder pads for in-line low pass & high pass filters.
7. The switch arrays connect to the *input side* of the relays in their respective relay banks. The outputs of the relay banks connect to the pins of the socket that holds the sample or to SMA daughter board.
8. There are two sets of switches to ground individual pins of the sample. One bank directly grounds the pins of the sample. The other connects to the SPout bus so grounds can be switched in and out during execution of a Test Definition.
9. There are six IN and OUT channels but 24 pins on the ZIF socket. Solder holes in the PCB allow connection of any pins of the socket to any of the six individual IN and OUT relay banks.

IN-A/IN-B Mux

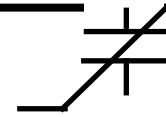


- It is expected that DRIVE and RETURN from the Radiant pMEMS Tester will be connected to IN-A and IN-B respectively.
- Experience has shown that the IN Switch Array configuration must change for different test formats. Measuring hysteresis loops is different than measuring direct piezoelectric response of capacitors.
 - 1) For hysteresis loops, DRIVE = Top electrode while RETURN = Bottom Electrode.
 - 2) For piezoelectric response, RETURN = top Electrode while GROUND = Bottom Electrode.
- IN-A and IN-B each have two independent switch banks selected independently by relays controlled by Vision.

The A/B Mux makes programming the Matrix Board more complex but allows a single setting of all switch banks to handle all possible test configurations for each pMEMS die type without changing switches *between tests*.



Vision Tasks



- Two Tasks control the Matrix Board in Vision
 1. The pMEMS Matrix Map Task
 2. The pMEMS Matrix Relay Task

- The Map Task is a passive Task that *records* the settings of all manual DIP switches on the board as well as the names of the signals and sample pins.
 1. Each Matrix Map may be saved as a file to be recalled by the Relay Task. (A direct connection would probably be better.)
 2. Each Map file ensures that the switch settings on the Matrix Board for a particular sample are saved *in the Vision DataSet* for future reference.

- The Matrix Relay Task is an active Task inserted into Test Definitions to close and open individual relays on the Matrix Board during test execution.

pMEMS Matrix Map Menu

- When a new map is created, the menu will be blank.

Matrix Map Menu

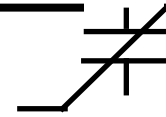
IN-A Name	A Bank 1 ○○○○○○○○ 1 2 3 4 5 6	A Bank 2 ○○○○○○○○ 1 2 3 4 5 6	1 Pin 1 Name	24	A Bank ○○○○○○○○ 1 2 3 4 5 6	OUT-A Name
IN-B Name	B Bank 1 ○○○○○○○○ 1 2 3 4 5 6	B Bank 2 ○○○○○○○○ 1 2 3 4 5 6	2 Pin 2 Name	12	B Bank ○○○○○○○○ 1 2 3 4 5 6	OUT-B Name
IN-C Name	C Bank ○○○○○○○○ 1 2 3 4 5 6		3 Pin 3 Name	7	C Bank ○○○○○○○○ 1 2 3 4 5 6	OUT-C Name
			4 Pin 4 Name	17		
			5 Pin 5 Name	18		
			6 Pin 6 Name	9		

All labels in **blue** are entered by the user.

FB 1 IN ○○○○○○○○ 1 2 3 4 5 6	Feedback Amp 1	FB 1 SPo ○○○○○○ 1 2 3 4 5 6	FB 1 OUT ○○○○ ABC i	Gnd SPo ○○○○○○ 1 2 3 4 5 6	Gnd Pins ○○○○○○ 1 2 3 4 5 6
FB 2 IN ○○○○○○○○ 1 2 3 4 5 6	Feedback Amp 2	FB 2 SPo ○○○○○○ 1 2 3 4 5 6	FB 2 OUT ○○○○ ABC i		

NOTES: *List external documentation or comments about use here.*

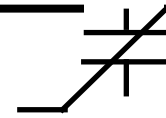
Pin Name Boxes



- The pMEMS Matrix Board has six (6) test channels but a 24-pin ZIF socket.
- Each test channel can be assigned to a name to prevent mistakes during programming.
- The **Black** number in the upper left of each name box is the Test Channel number.
- The **Blue** number in the upper right of the name box is the pin number of the ZIF socket to which that Test Channel is connected by a soldered wire.

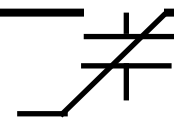
1		24
	Pin 1 Name	
2		12
	Pin 2 Name	
3		7
	Pin 3 Name	
4		17
	Pin 4 Name	
5		18
	Pin 5 Name	
6		9
	Pin 6 Name	

Examples



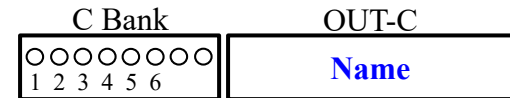
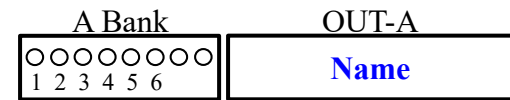
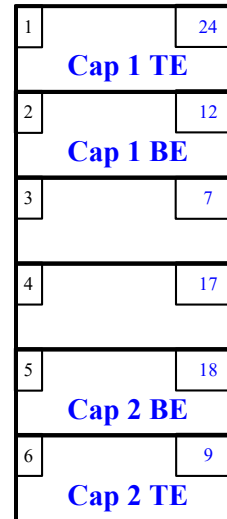
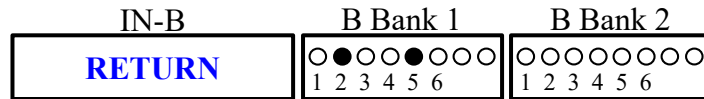
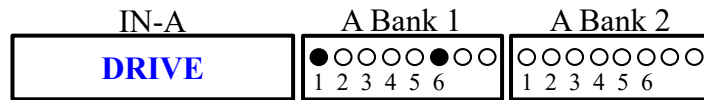
- Two examples for configuring the pMEMS Matrix Map follow.
- Map 1: a single package containing two independent capacitors.
 1. Only electrical measurements such as Hysteresis loops, Leakage tests and PUND measurements are to be executed on this package.
 2. Only connections to the DRIVE and RETURN of the tester are needed.
- Map 2: two capacitors used as sensors on independent cantilevers.
 1. The cantilevers act as accelerometers.
 2. The two cantilevers are ferroelectric and must be tested prior to use.
 3. When the cantilevers are disturbed by motion, they flex the piezoelectric capacitors which in turn generate voltage.
 4. OUT amplifiers A and B amplify the sensor capacitor voltages and output them to the Sensor1 and Sensor2 inputs of the tester.
- In both examples, the Matrix Board is configured only once for all tests in the sequence.

Example Map 1

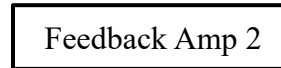
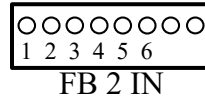
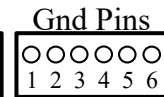
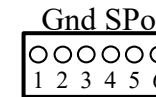
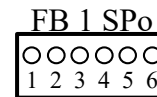
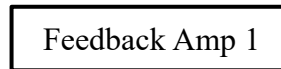
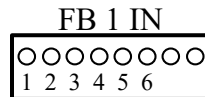


Two simple capacitors together in a package configured for hysteresis testing.

Matrix Map Menu

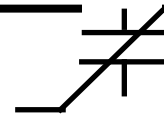


*See
comments
next page.*



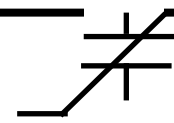
NOTES: *List external documentation or comments about use here.* **This is a standard Task Comments control.**

Comments on Map 1



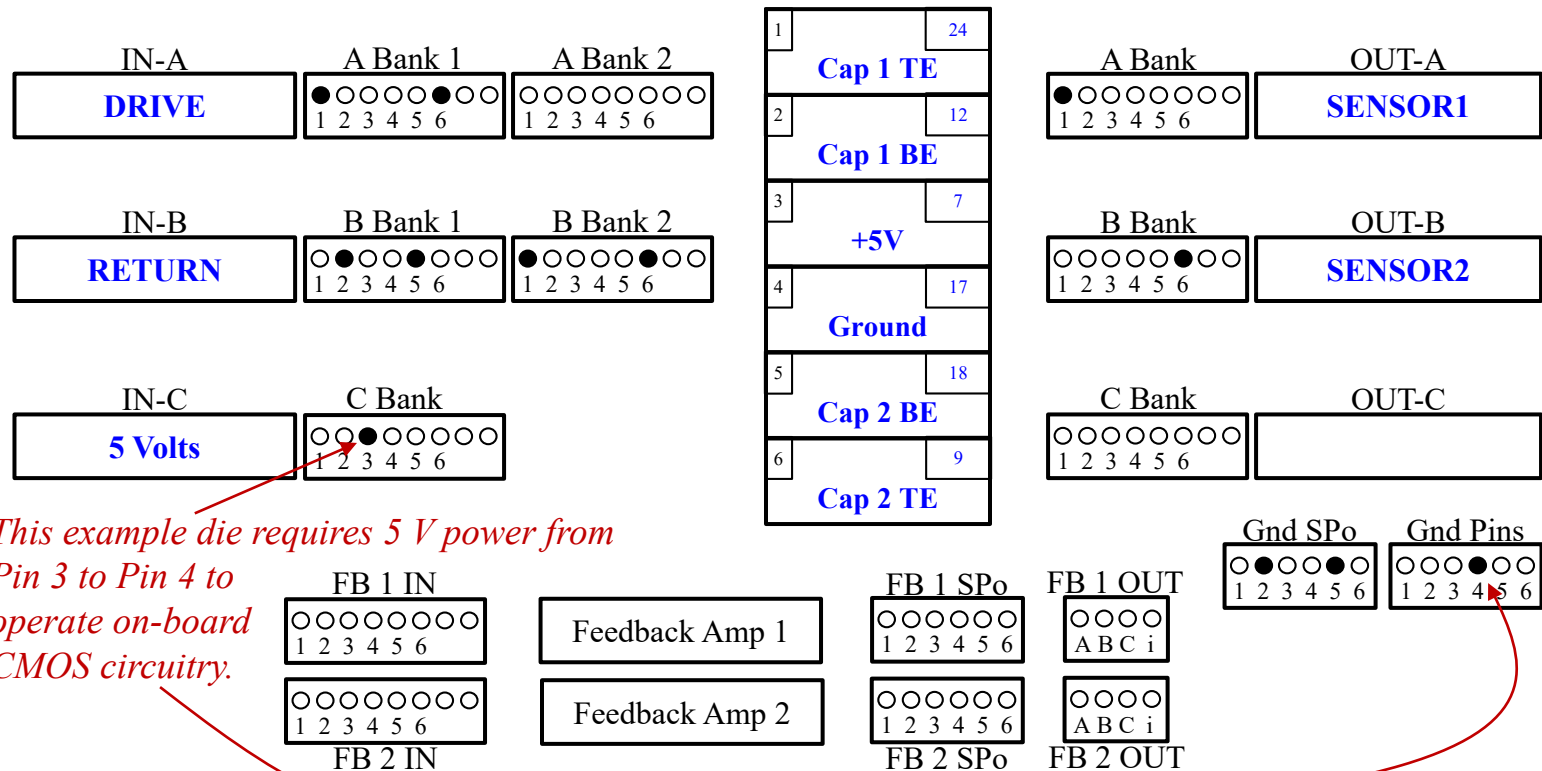
- In the simple example Map 1 of the previous page:
 1. The sample has only two capacitors.
 2. The **DRIVE** signal from the tester should be connected to **IN-A** while **RETURN** should be connected to **IN-B**.
 3. BNC **IN-A1** switches are set so that if **Relay SP1i** is closed, **DRIVE** will be connected to **Pin 1** of the sample.
 4. BNC **IN-A1** switches are also set so that if **Relay SP6i** is closed, **DRIVE** will be connected to **Pin 6** of the sample.
 5. If both **Relays SP1i & SP6i** are closed at the same time, **DRIVE** will be connected to both **Pin 1** and **Pin 6** at the same time, for instance to do poling.
 6. The **IN-B1** switches are set so that **Relay SP2i** will connect the **RETURN** to the bottom electrode of **Capacitor 1** while **Relay SP5i** will connect **RETURN** to the bottom electrode of **Capacitor 2**.
 7. BNC **IN-C** has no connections.
 8. No **OUT** signals and no **Feedback** signals are connected to the sample.

Example Map 2



Two piezoelectric actuators configured for hysteresis loops & direct piezo sensing.

Matrix Map Menu



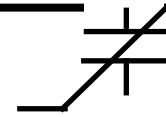
This example die requires 5 V power from Pin 3 to Pin 4 to operate on-board CMOS circuitry.

NOTES: *List external documentation or comments about use here.*

Comments on Map 2

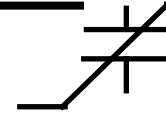
- Map 2 allows Hysteresis testing from the left then sensing of the cantilever piezoelectric signals to the right using the SENSOR ports of the tester:
 1. The **Map 2** adds more connections to **Map 1**.
 2. Using **IN-A1 & IN-B1**, execute the Hysteresis loops as described for **Map 1**. Then execute Monopolar loops to orient each capacitor UP towards its TE or DOWN towards its BE.
 3. Close **Relay SP3i** to connect 5V to the **Pin 3** of the die. **Pin 4** of the die is **hard grounded**. (This theoretical die needs 5 volts.)
 4. Switch to the **IN-A2** and **IN-B2** switch banks. Turn on **SP1i** to connect **Capacitor 1 TE** to **RETURN**. Turn on **SP2o** to connect **Capacitor 1 BE** to **ground**. Physically stimulate **Cantilever 1** while running **All Zeros Hysteresis Task**. The tester **RETURN** will capture piezoelectric charge from Capacitor 1 due to physical stimulus of the cantilever.

Map 2 continued



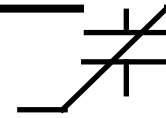
5. To capture outputs of both cantilevers simultaneously during physical stimulation, open all IN relays. Close **Relays SP1o & SP2o** to connect the TE of both capacitors to OUTA and OUTB respectively through their amplifiers. Close **Relays SP2o & SP5o** to connect the bottom electrodes of both capacitors to ground. Physically stimulate both cantilevers while running **All Zeros Hysteresis** or **Sensor Oscilloscope** Tasks to see the sensor response.

Saving Map Files



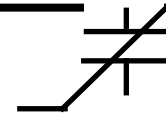
- pMEMS Map settings may be saved to Map files.
- The pMEMS Matrix Board Relays Task can recall Map files to fill in signal and die pin names when the relays are programmed.

Signal Names



- When a manual Switch is set in the Map Task menu, Vision will transfer the name associated with that switch to the appropriate location on the map representing the board.
- There are seventeen (17) names that can appear on a pin of the sample, on the input of a feedback amplifier, an output of a feedback amplifier, or an input to an OUT signal.
 1. The name of the signal attached to IN-A
 2. The name of the signal attached to IN-B
 3. The name of the signal attached to IN-C
 4. The name of the signal attached to OUT-A
 5. The name of the signal attached to OUT-B
 6. The name of the signal attached to OUT-C
 7. Ground
 8. FAPin1 (Feedback Amplifier Path 1 Input)
 9. FAPin2 (Feedback Amplifier Path 2 Input)
 10. FAPout1 (Feedback Amplifier Path 1 Output)
 11. FAPout2 (Feedback Amplifier Path 2 Output)
 12. Any of the six names assigned to the pins of the sample.
- Vision will perform error checking of the settings. All errors must be corrected before Vision will allow the Map file to be loaded to a Relay menu.

Matrix Map Errors



1. Assigning two IN signals (A, B, or C) to the same relay.

Example: IN-A and IN-C cannot both be assigned to SP1in. That would short them together. The exception is that SP1i of Switch Bank 1 is independent of SP1i of Switch Bank 2 of the IN-A and IN-B inputs. The other SPin lines follow suit.

2. No signal can be assigned to a pin that is also assigned to GND.

Example: IN-B assigned to SP3i when Pin3 of the sample is connected to GND is not allowed.

3. A feedback output cannot be assigned back to the same pin as its input.

4. The output of an OUT amplifier cannot be assigned to the same Cable Driver input if the output of a feedback amplifier is also assigned to that driver.

Example: FAPout1 and the OUT-A amplifier cannot both be assigned to the OUT-A cable driver.

Additional Resources

- The pMEMS Matrix Board has additional functions not described in this document.
- Some DIP switch banks have 8 switches, two more than the six test channels they are connected to. The extra two switches add extra connection paths or differential signals into amplifiers.
- There are two DACs embedded in the feedback paths to enable DC level shifting of feedback voltages.
- You must review the circuit diagram for the Matrix Board in order to use its more complex functions.
- The full circuit diagram for the Matrix Board can be called up from a button on the MAP menu.
- Contact Radiant Technologies with questions.

pMEMS Relay Task

- The pMEMS Matrix Board Relays Task opens and closes relays on the Matrix Board when called from QuikLook or inside a Test Definition.
 1. Each check boxes on the menu represents a relay on the Matrix Board.
 2. A few, all or no relays may be selected when the Task executes.
 3. The menu has windows for labeling signals on the board.
 4. The Relay Task will execute with the labels left blank.
 5. A pMEMS Map file can be recalled to the Relay menu.
 1. Upon recall, Vision will read the Map file and assign labels to the IN and OUT BNCs as well as the *input* of each relay.
 2. When a relay is closed, Vision will transfer the label of that relay to its output.
 3. When used in conjunction with the Map files, the Relay Task will display the signal routing by name to/from the device under test.
 6. The Relay Task provides controls to create a sequence of relay conditions when the Task is embedded inside a Branch Loop.

pMEMS Relay Task

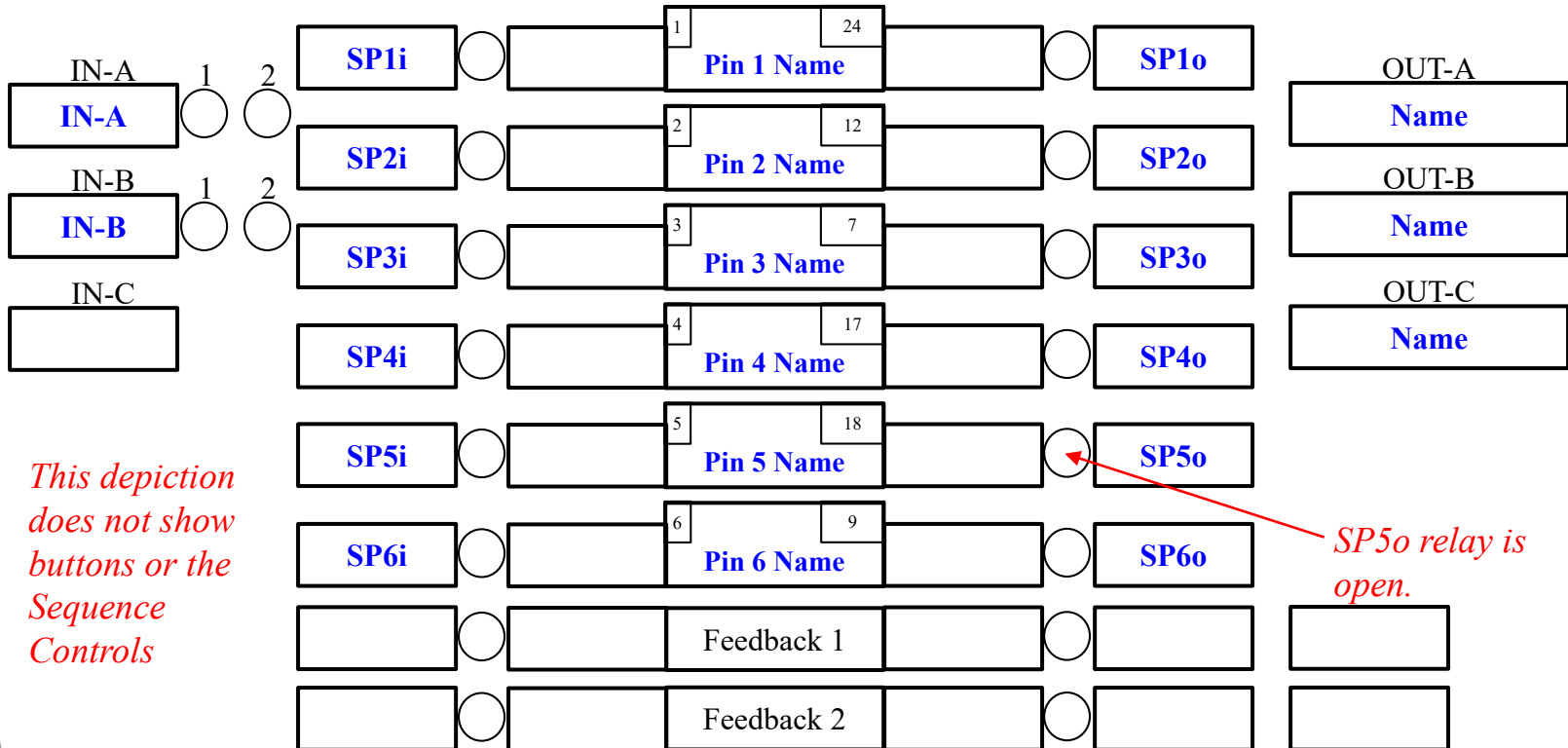
- The blank menu is shown below. It is functional without labels.

Matrix Relay Menu

No Map

Recall Map File

Open Map File

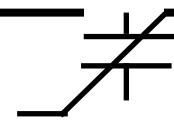


This depiction does not show buttons or the Sequence Controls

SP5o relay is open.

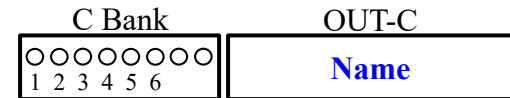
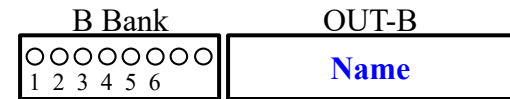
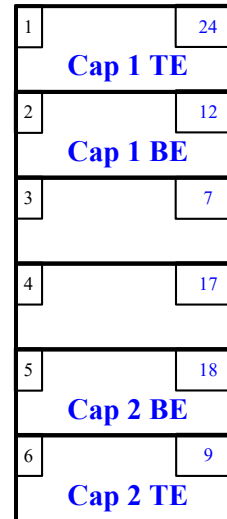
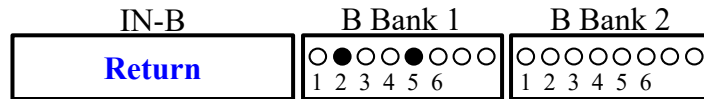
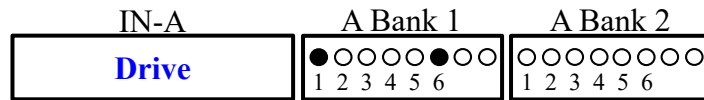
NOTES: List external documentation or comments about use here.

Example Map 1

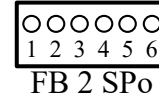
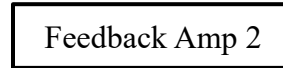
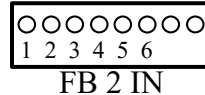
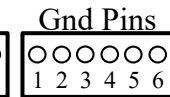
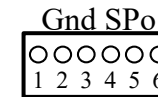
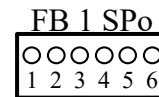
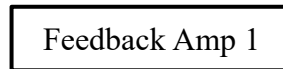
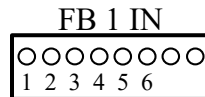


Two simple capacitors together in a package configured for hysteresis testing.

Matrix Map Menu



*See
comments
next page.*



NOTES: *List external documentation or comments about use here.*

pMEMS Relay Task

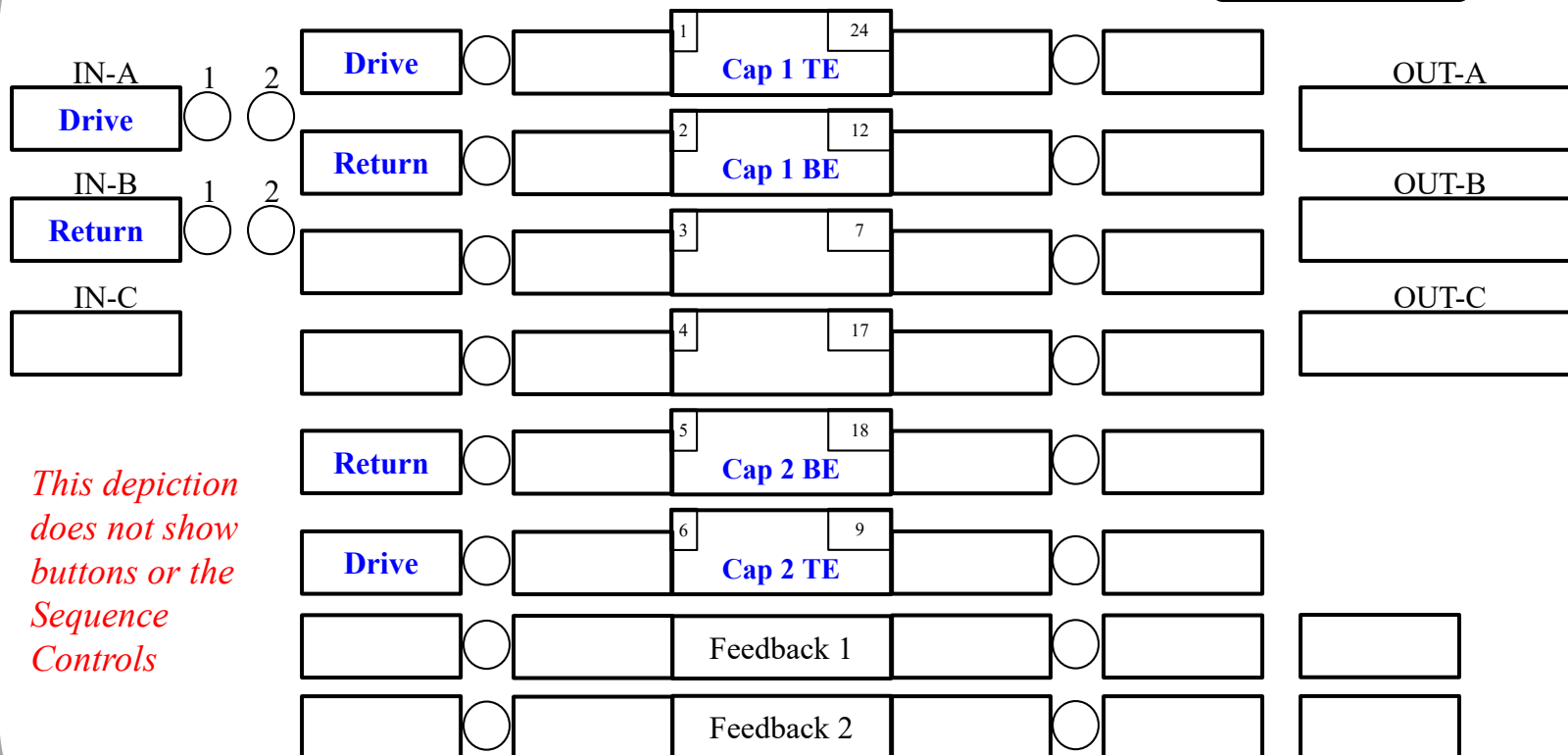
- Recalling the Map 1 file fills in all labels.

Matrix Relay Menu

Recall Map File

Open Map File

Map 1



This depiction does not show buttons or the Sequence Controls

NOTES: List external documentation or comments about use here.

pMEMS Relay Task

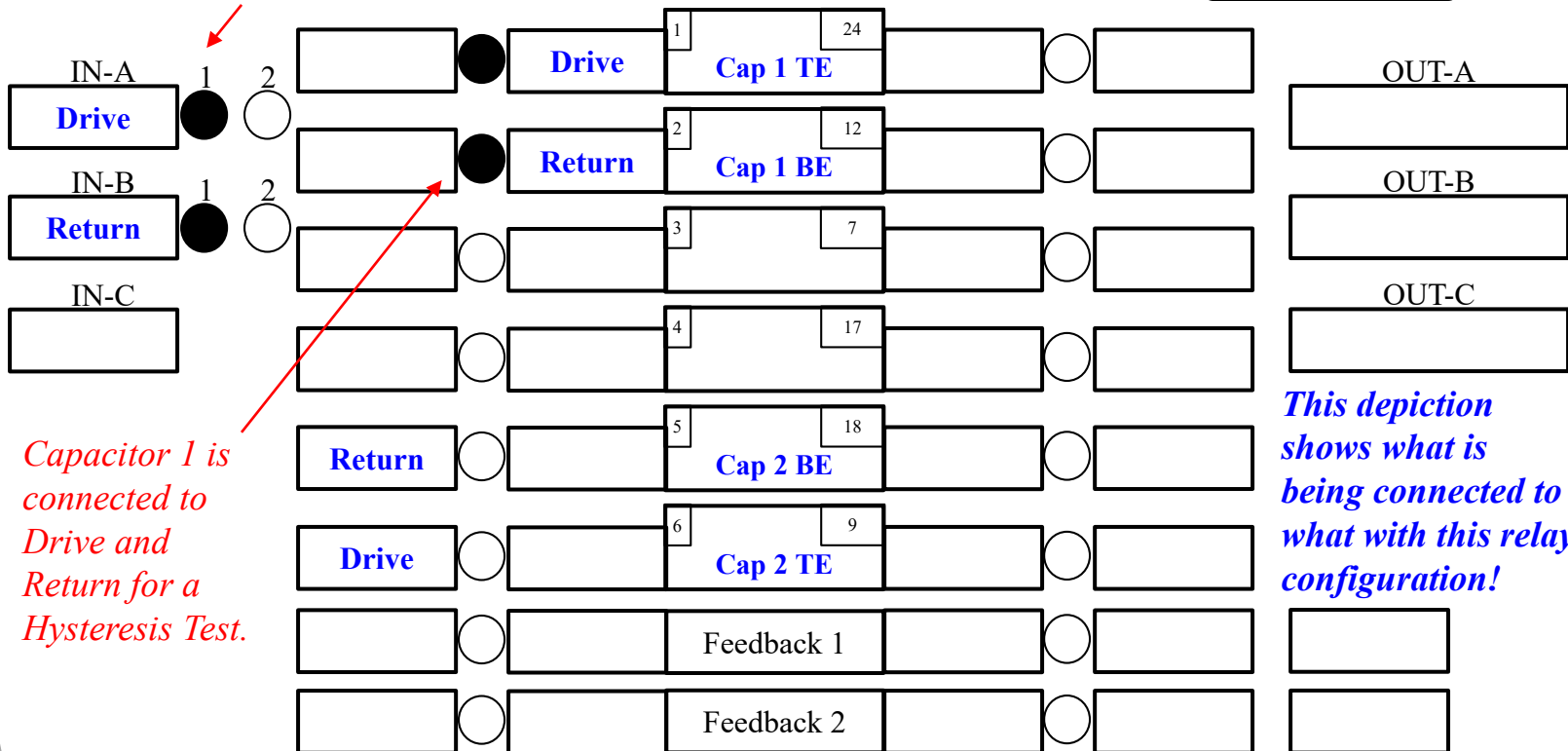
- Setting relays transfers the labels to the pins of the sample.

Matrix Relay Menu

Recall Map File
Open Map File

Map 1

Banks A1 & B1 selected.



NOTES: List external documentation or comments about use here.

pMEMS Relay Task

- Change relay settings to test Capacitor 2.

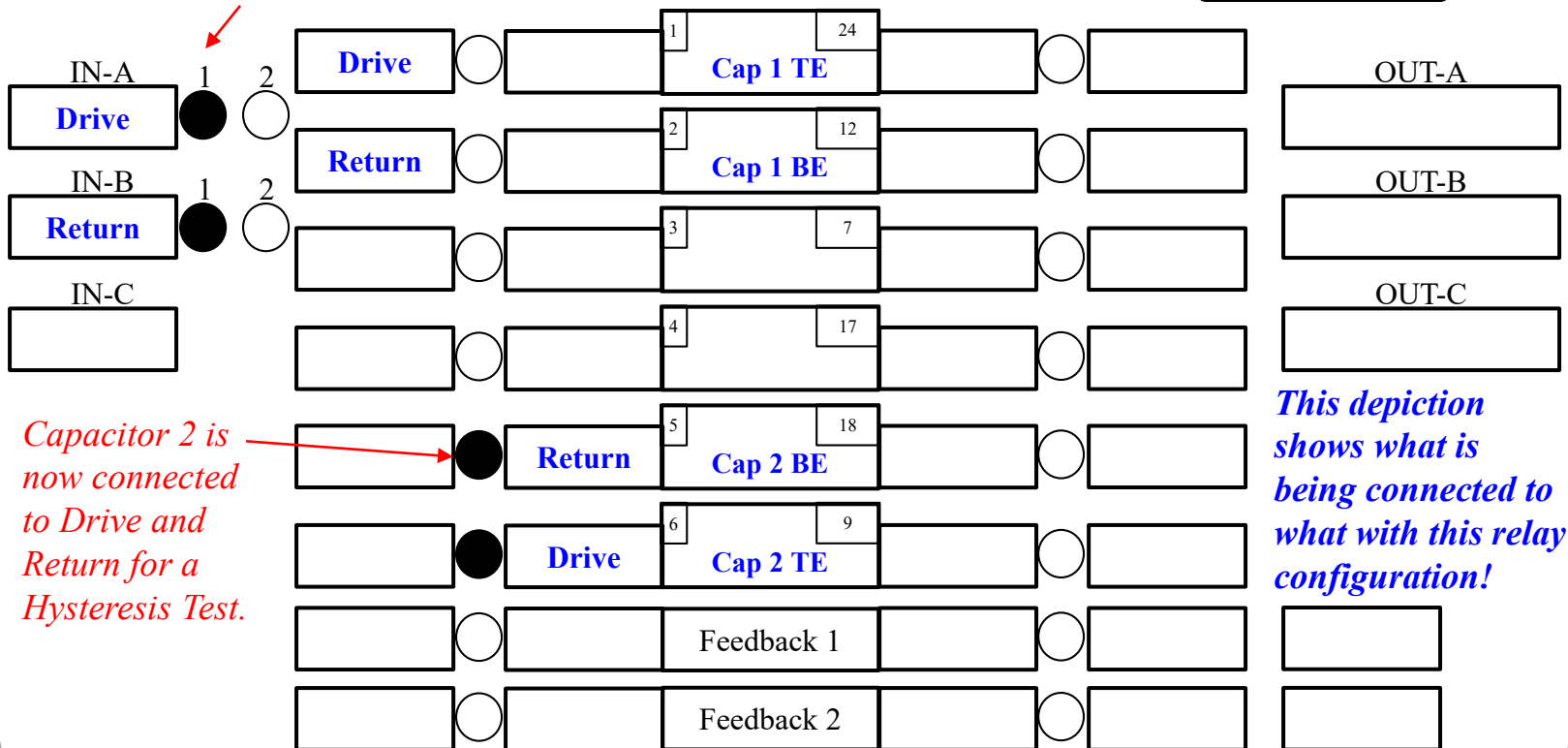
Matrix Relay Menu

Recall Map File

Open Map File

Map 1

Banks A1 & B1 selected.

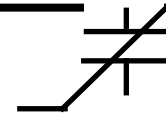


Capacitor 2 is now connected to Drive and Return for a Hysteresis Test.

This depiction shows what is being connected to what with this relay configuration!

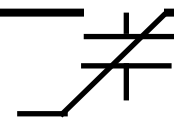
NOTES: List external documentation or comments about use here.

Create New Maps



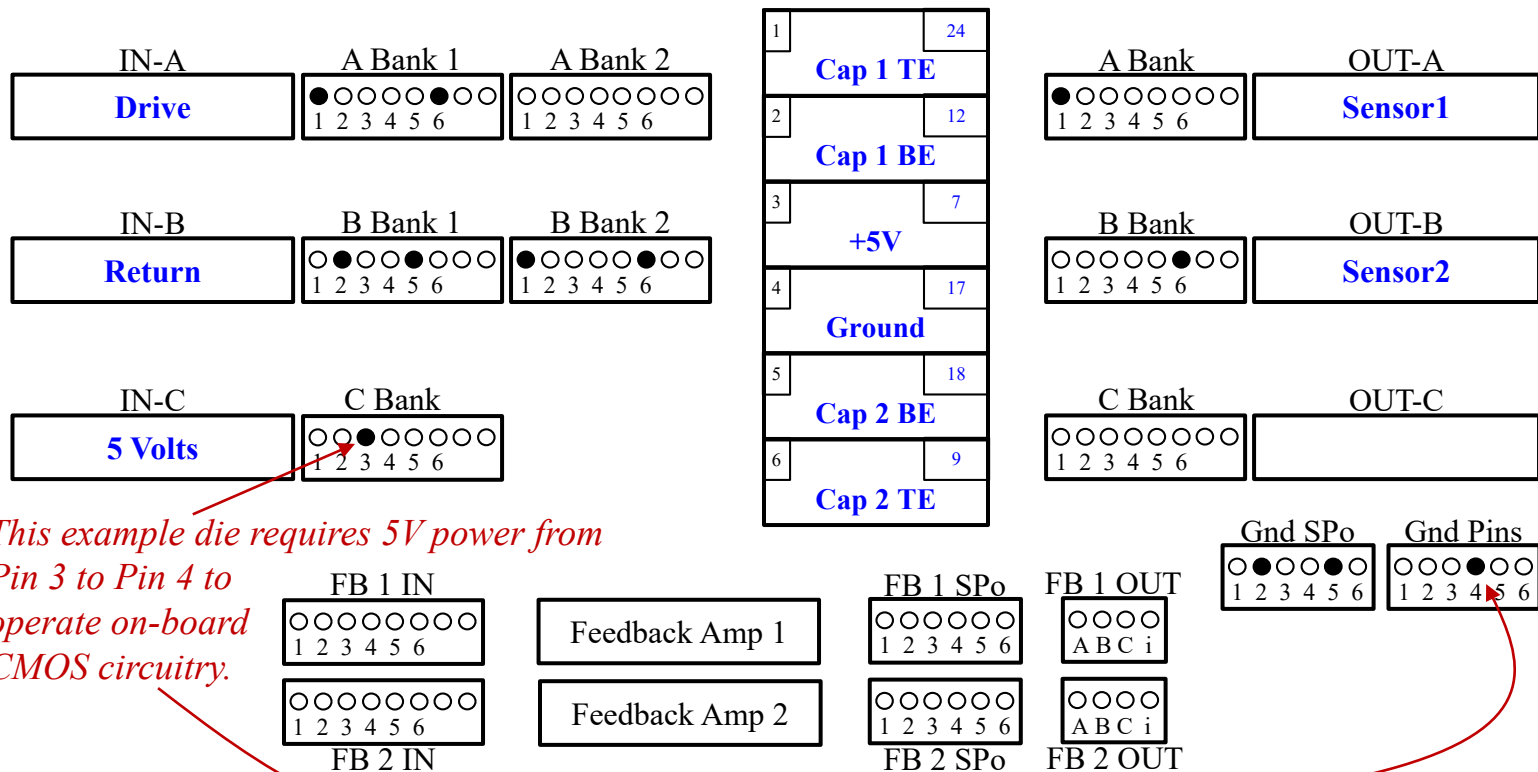
- Modify Map 1 with additional connections so that after the hysteresis tests are completed the oscillations of the capacitors are amplified and sent to the test Sensor inputs.
- Save this modified Map file as Map 2.
- Add a feedback path and save it as Map 3.

Example Map 2



Two piezoelectric actuators configured for hysteresis loops & direct piezo sensing.

Matrix Map Menu



This example die requires 5V power from Pin 3 to Pin 4 to operate on-board CMOS circuitry.

NOTES: *List external documentation or comments about use here.*

pMEMS Relay Task

- OUT relays are added to the configuration.

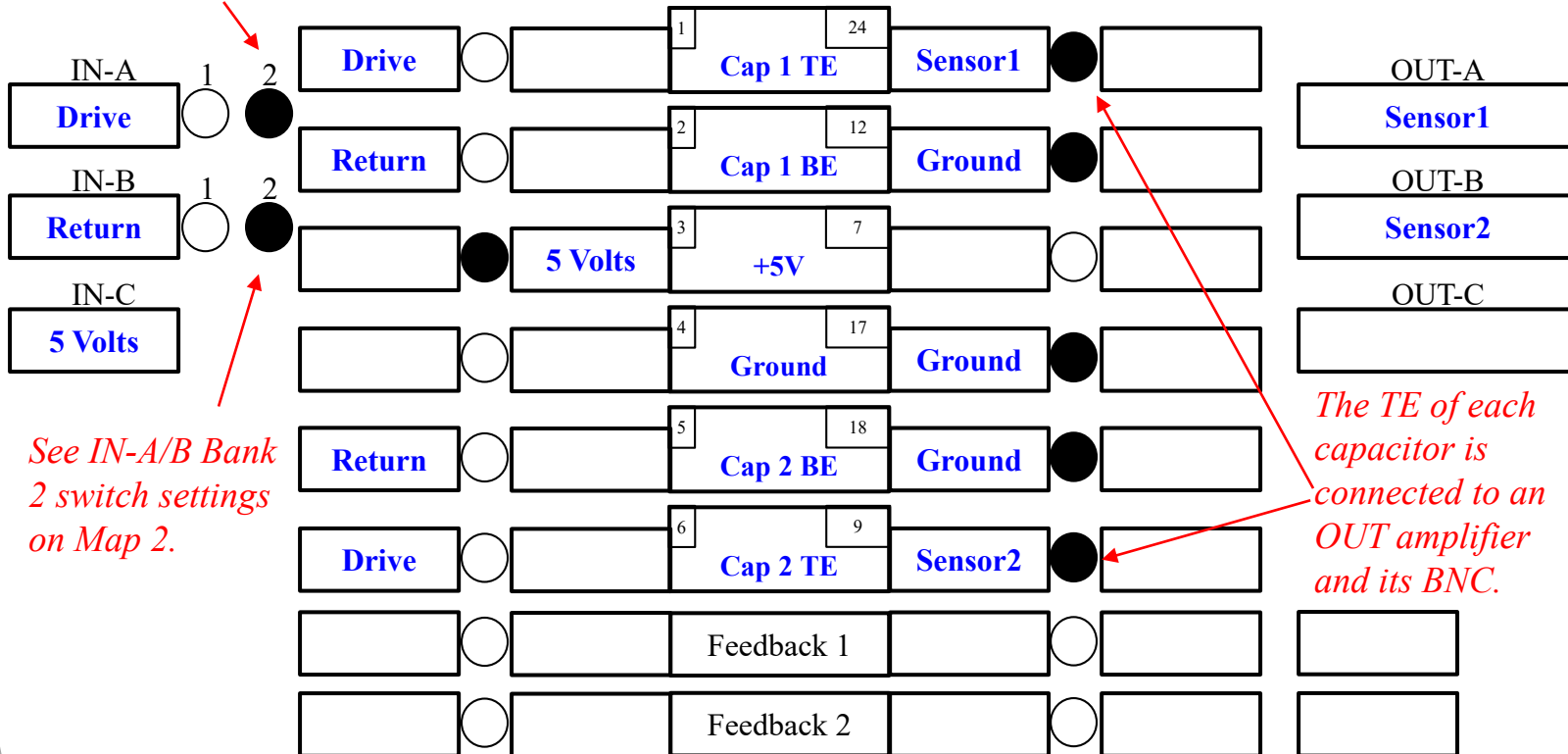
Matrix Relay Menu

Recall Map File

Open Map File

Map 2

Banks A2 & B2 selected.

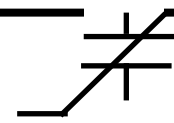


See IN-A/B Bank 2 switch settings on Map 2.

The TE of each capacitor is connected to an OUT amplifier and its BNC.

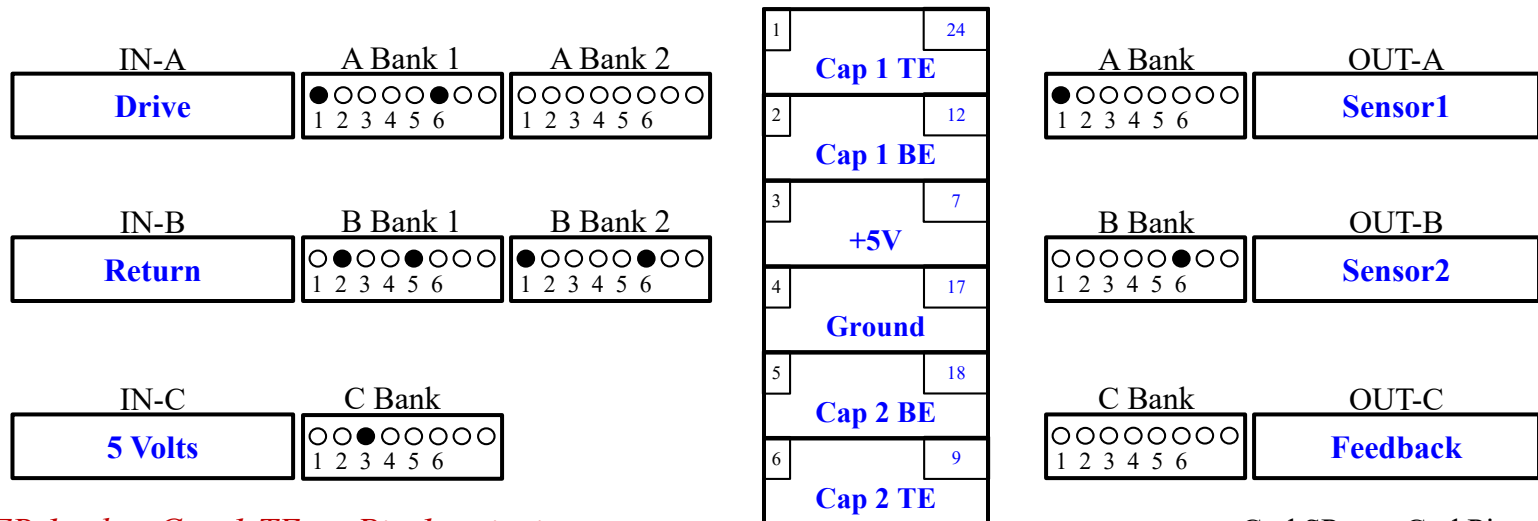
NOTES: List external documentation or comments about use here.

Create Map 3

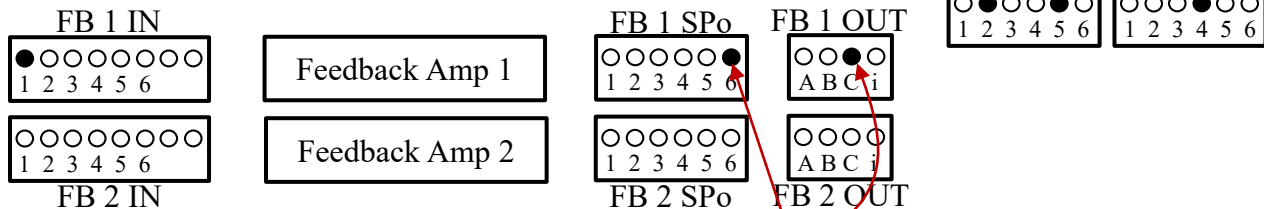


Add feedback from Pin 1 to Pin 6 to change Map 2 to Map 3.

Matrix Map Menu



FB 1 takes Cap 1 TE on Pin 1 as its input and outputs to Pin 6. It also outputs its signal directly to Cable Driver C.



NOTES: List external documentation or comments about use here.

pMEMS Relay Task

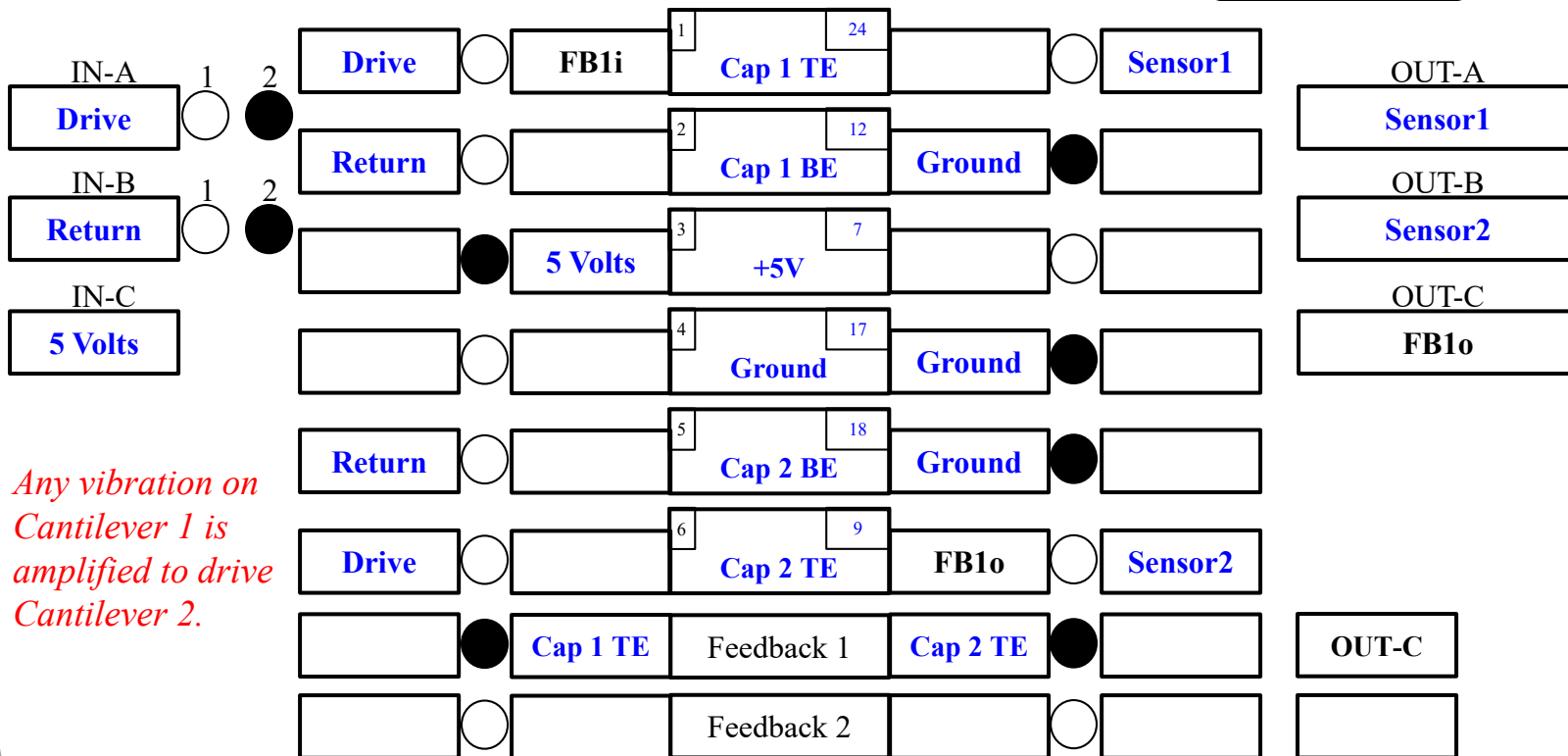
- Setting relays for feedback test using Map 3.

Matrix Relay Menu

Map 3

Recall Map File

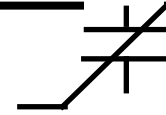
Open Map File



Any vibration on Cantilever 1 is amplified to drive Cantilever 2.

NOTES: List external documentation or comments about use here.

Summary

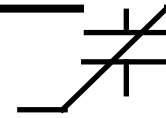


- The pMEMS matrix Board is quite complex but allows the device under test to be evaluated in multiple ways.
 - 1) Configure the switches.
 - 2) Fill in the Map.
 - 3) Set the Relays.
 - 4) Insert the device to test.
 - 5) Test.

Configuration Procedure

- **Determine** all tests to be executed.
- **Establish external connections** to be made to IN-A, IN-B, IN-C and OUT-A, OUT-B, and OUT-C for all tests.
- **Set the Switches** to route signals to the relay banks.
- **Open the pMEMS Matrix Map Task.**
 - 1) Enter the names of each pin of the sample
 - 2) Enter the signal names attached to the IN and OUT BNCs
 - 3) Enter the Switch settings
 - 4) Save the Matrix Map.
- **Insert the pMEMS Matrix Relay Task** at the appropriate points in the test.
 - 1) Recall the desired Matrix Map for that sample. When loaded, the names of the pins will appear on the sample diagram and the names of the external signals will appear on the inputs to the relay banks as determined by the Switch settings in the recalled Map.
 - 2) When relays are set to be closed by the Task, the appropriate signal name will appear at the assigned pin of the sample.
 - 3) Remember to open all relays at the end of each Test Definition.
- **Load the sample and run** the targeted tests.

Recall Map File



- A Map may be created and saved as an independent file using the pMEMS Map Task.
- A Map file may be loaded into the pMEMS Matrix Board Relays Task where it will insert the names of all signals and sample pin assignments.
- Once recalled into the pMEMS Relay Task, the Map itself can be opened, modified and re-saved.

Sequence Programming

- The pMEMS Matrix Board Relays Task has a section that records the relay configuration to be executed when the Task is called inside a Test Definition.
- Multiple configurations may be entered such as in the figure below to be executed in sequence as the Task is called multiple times within a Branch Loop.

*This sequence
executes Map 3.*

pMEMS Matrix Board Relays Configuration

pMEMS Matrix Relays Task Name (60 Characters Max.)
pMEMS Matrix Relays: 1

No Execute

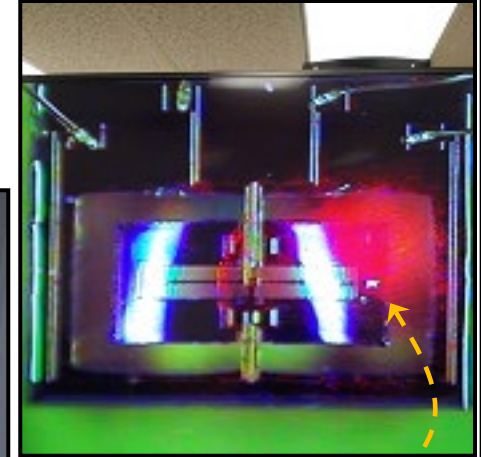
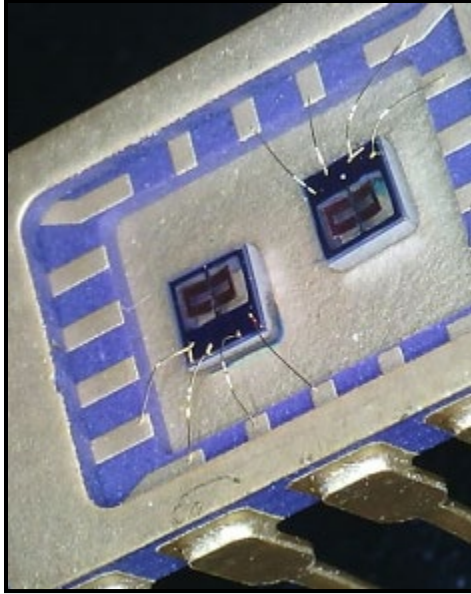
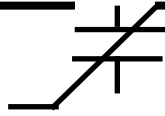
Relay Sequence List

SP1i - SP2i -
SP5i - SP6i -
SP3i - SP1o - SP2o - SP4o - SP5o - SP6o -
SP3i - WR1o - SP2o - SP4o - SP5o - WR1i -

Measuring Piezoelectrics

- The enclosure of the pMEMS Matrix Board is sized to fit under the Polytec NLV laser doppler vibrometer (LDV).
 1. A port through the top cover of the enclosure is positioned directly over the ZIF socket to allow the laser to see the entire are of the device under test.
 2. The enclosure will mount on an X:Y:Tip:Tilt table beneath the laser to position the laser split and align it back into its sensor.
- The NLV can measure displacements down to 0.2 Ångstroms and up to the millimeters when connected to a Radiant Premier II, Multiferroic II, or pMEMS tester.
- The NLV is fully compatible with Radiant's Vision operating system.
- With the NLV connected to the tester SENSOR ports while the tester operates the sample on the pMEMS Matrix Board, the direct and converse piezoelectric response of the devices under test will be captured simultaneously with the electrical measurements of the sample.

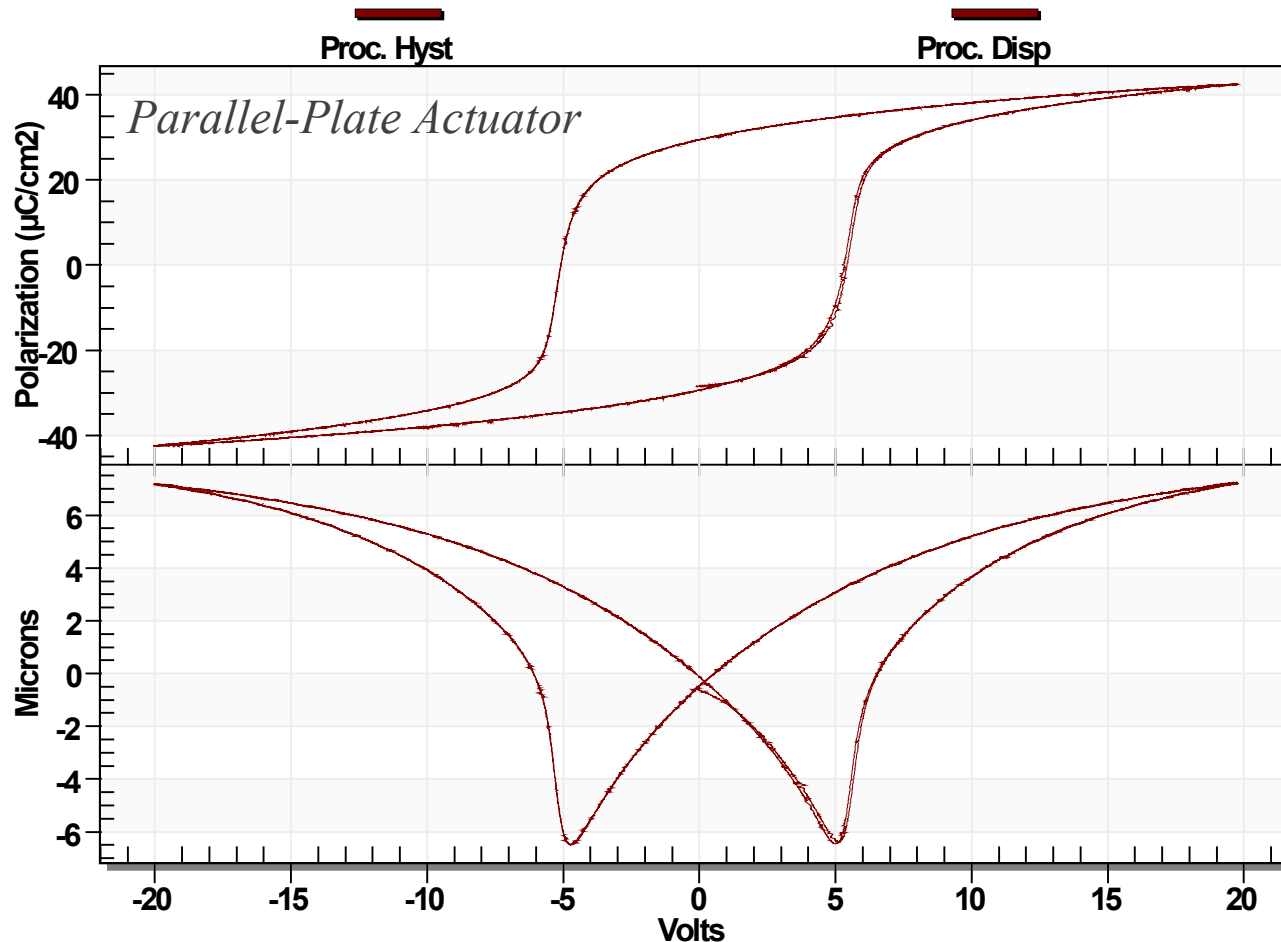
Measuring with LDV



LDV laser

- Measuring piezoelectric “wings” with an LDV.
- *This experiment in 2017 lead to the development of the Matrix Board.*

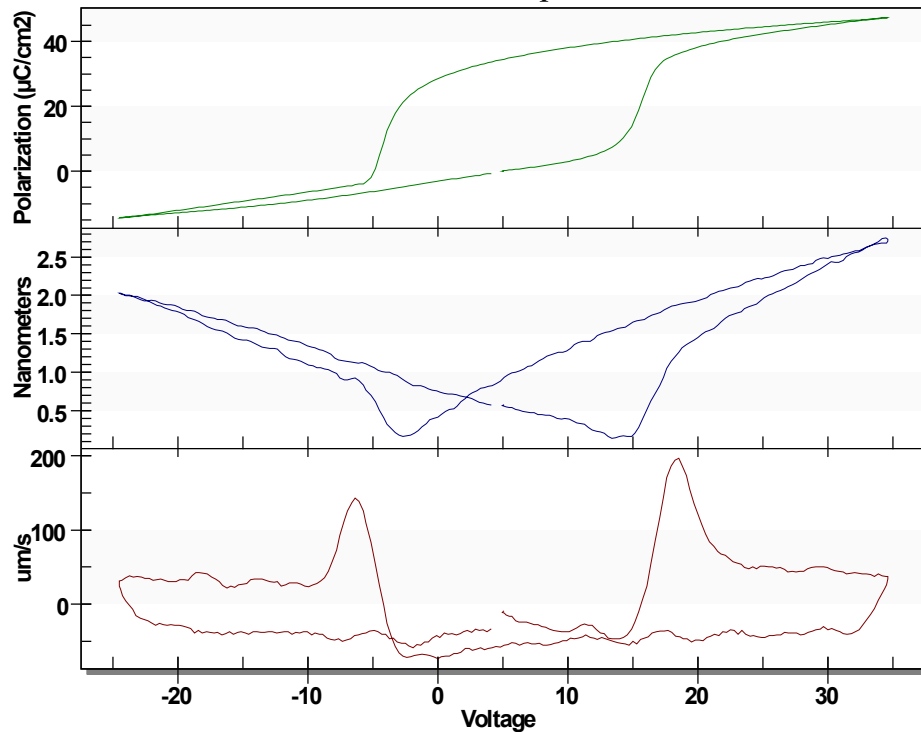
Motion of the Wings



- Double butterfly loop of wing on previous page driven by parallel-plate capacitors at 1Hz/20V with 32,000 points.

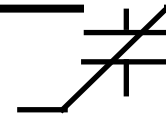
Angstrom Resolution

RTI 1 μ m PNZT Capacitor

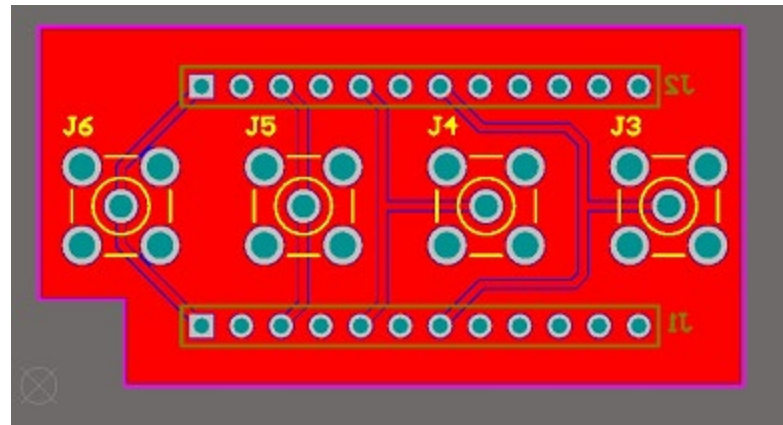


- 20 Å butterfly motion of the top surface of a 1 μ m-thick parallel-plate PNZT capacitor clamped to the substrate surface.
- The pMEMS Matrix Board mounted beneath the Polytec NLV laser vibrometer is a powerful tool for measuring complex piezoMEMS.

Using Cables



- The ZIF socket on the pMEMS Matrix Board will hold 300 mil to 600 mil DIP packages or printed circuit boards having headers positioned to fit DIP footprints.
- A special daughter board provided by Radiant for the Matrix Board locks into the ZIF socket and holds four SMA connectors.
- Using SMA-to-BNC cables, the daughter board allows the Matrix Board to test devices on a probe station, in a thermal chamber, or in arrays controlled by multiplexers.

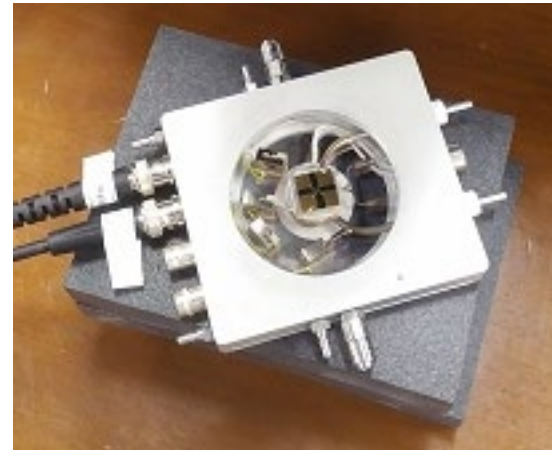


Testing at Temperature

- Using the pMEMS SMA Daughter Board, four test channels of the Matrix Board may be connected to small thermal chambers from Instec and Linkam.



Instec HCP621G-PM

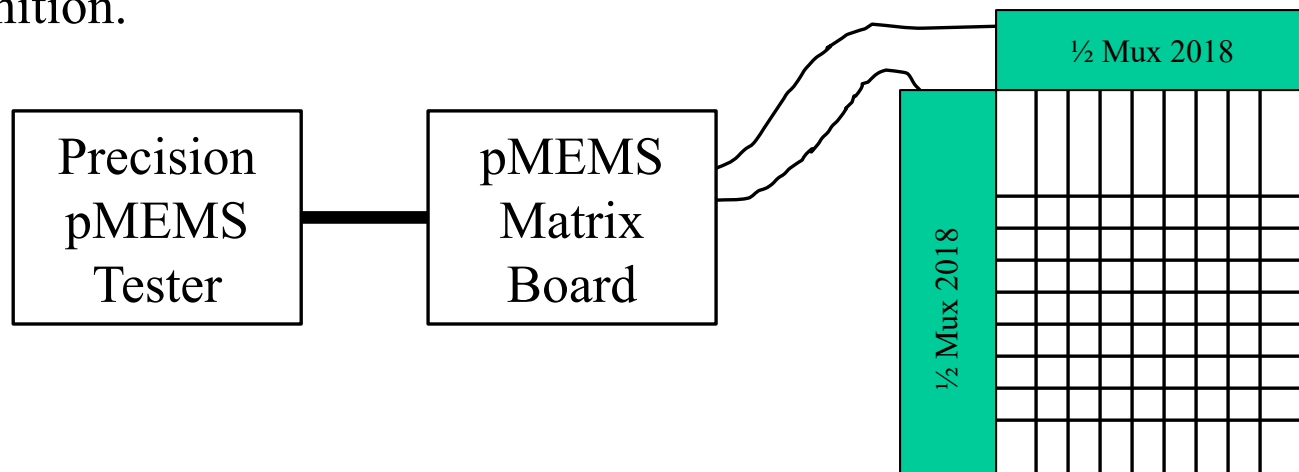


Linkam HFS600E-P

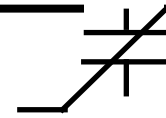
- These chambers sit on a table top but will take the sample from -190°C up to 600°C . They have connections for four electrical signals between the tester through the Matrix board to the sample inside the chamber.
- The chambers interface with the NLV laser & are fully controllable by Vision.

Adding Multiplexers

- Radiant Technologies offers the Precision Multiplexer 2018 controlled from within Vision.
- The multiplexer has two independent 1x8 multiplexers.
- Vision will control up to three multiplexers at a time.
- Connecting two SMA-to-BNC cables from the pMEMS Matrix Board to the Multiplexer 2018 allows full testing of cross-point arrays up to 8x8. Two Mux 2018s will scan 16x16 arrays in a Vision Test Definition.

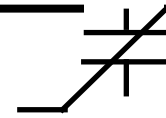


Testing Transistors



- The Precision pMEMS Tester is a fully functional analog ferroelectric tester with additional channels to test semiconductor devices made with PVDF or ferroelectric ceramic gates.
- In addition to a Frequency Counter, Parallel DIO channel, I²C comm channel, and an LCR, the pMEMS Tester hosts two asynchronous 16-bit voltage sources (V1 & V2) and one asynchronous 16-bit ADC.
- The connections from the tester to a FET or a diode are
 1. DRIVE = Gate
 2. RETURN= Source
 3. V2 = Drain
 4. V1 = Substrate bias
- Connected to the Matrix Board, the pMEMS transistor test signals easily switch between Curve Trace and Ids vs Vgs test configurations for multiple transistors on a single die.

Conclusion



- Radiant ferroelectric and piezoelectric test instruments have proven themselves accurate and versatile for characterizing individual non-linear capacitors.
- Multiple non-linear capacitors are now being fabricated on membranes, cantilevers, and beams of piezoMEMS systems-on-chip. SOCs require complex test sequences.
- Radiant's pMEMS Matrix Board is a unique accessory containing manual switches, Vision-controlled relays, and on-board amplifiers to interface a packaged pMEMS SOC with a Radiant tester for functional system testing.
- The Matrix Board will also connect to unpackaged SOCs on probe stations, thermal chambers, multiplexers, and laser interferometers